# KPN005SS-ZBw2

**512MB LP-DDR2**

**CONFIDENTIAL**
**DO NOT DISCLOSE**



This is preliminary document release.

All specifications are subject to change without notice.

The material contained in this document supersedes all previous documentation issued for the related products included herein. Please contact Leahkinn for the latest document(s).

All sales are subject to Leahkinn's Standard Terms and Conditions

http://www.leahkinn.com

# 4Gbits Mobile DDR2

## Poduct Features

- Density: 4G bits
- Organization
  - ×32 bits: 16M words × 32 bits × 8 banks
- Package:
  - 168 ball
  - Area: 12 × 12mm
  - Height: 0.8mm (max)
  - Ball Pitch: 0.5mm
- Power supply
- VDD1 = 1.70V to 1.95V
- VDD2, VDDQ, VDDCA = 1.14V to 1.30V
- Data rate: 800Mbps max. (RL = 6)
- 4KB page size
  - Row address: R0 to R13
  - Column address: C0 to C9 (× 32 bits)
- Eight internal banks for concurrent operation
- Interface: HSUL_12
- Burst lengths (BL): 4, 8, 16
- Burst type (BT)
  - Sequential (4, 8, 16)
  - Interleave (4, 8)
- Read latency (RL): 3, 4, 5, 6, 7, 8
- Precharge: auto precharge option for each burst access
- Programmable driver strength
- Refresh: auto-refresh, self-refresh
- Refresh cycles: 8192 cycles/32ms
  - Average refresh period: 3.9μs
- Operating junction temperature range
  - TJ = -30°C to +85°C
- DLL is not implemented
- Low power consumption
- JEDEC LPDDR2-S4B compliance
- Per Bank Refresh
- Partial Array Self-Refresh (PASR)
  - Bank Masking
  - Segment Masking
- Auto Temperature Compensated Self-Refresh
- (ATCSR) by built-in temperature sensor
- Deep power-down mode
- Double-data-rate architecture; two data transfers per one clock cycle
- The high-speed data transfer is realized by the
- 4 bits prefetch pipelined architecture
- Differential clock inputs (CK and /CK)
- Bi-directional differential data strobe (DQS and /DQS)
- Commands entered on both rising and falling CK edge; data and data mask referenced to both edges of DQS
- Data mask (DM) for write data
- Burst termination by burst stop command

# Table of Contents

# Tables

# Figures

# 1.0 Introduction

This document contains the specifications for 512MB (SDP) LP-DDR2 Memory.

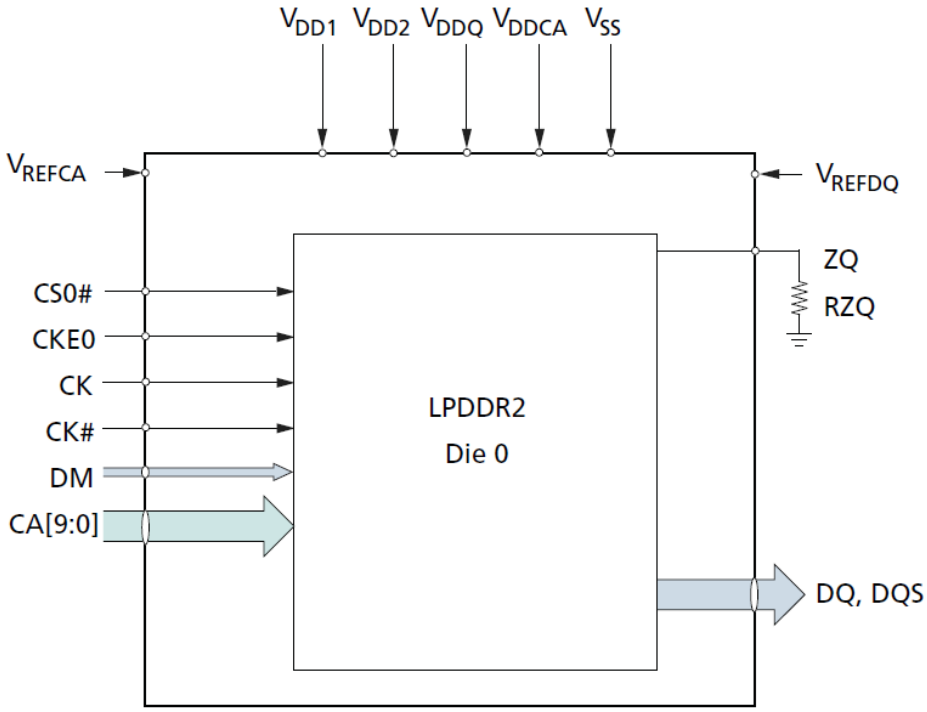
## 1.1 Product Overview

The product targets for mobile phone & tablets applications with low-power, high-performance, and minimal package-footprint design requirements.

We offer 512MB density with the same & compatible package.

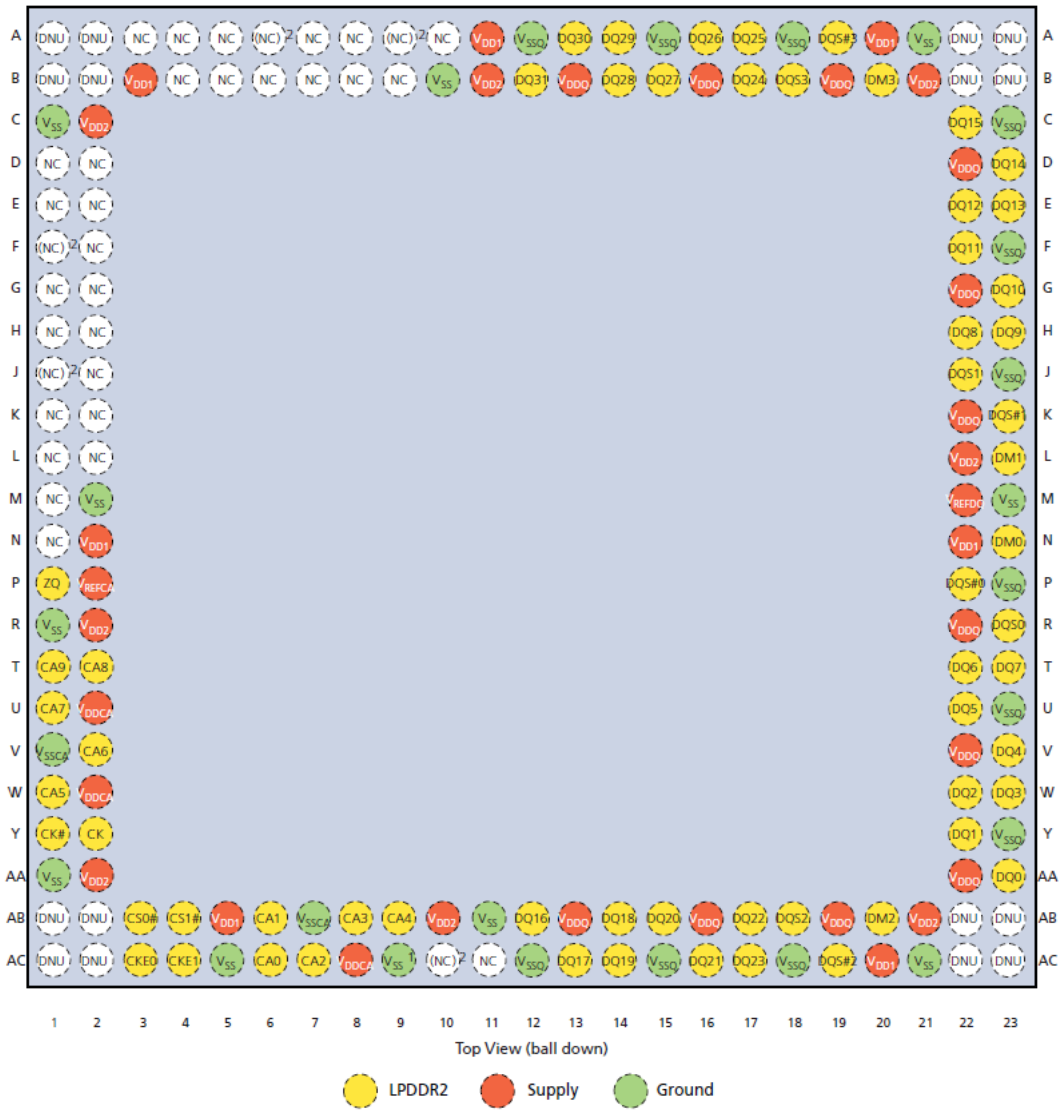
## 1.2 Block Diagrams

Figure 1. Single die Block Diagram



## 1.3 Package Ballout

Figure 2. 168-Ball TFBGA (LP-DDR2 x32) Ball Assignment




Notes: 1. Ball AC9 may be $V_{SS}$ or left unconnected.
2. Balls labeled NC = no connect; however, they can be connected together internally.

## 1.4 Signal Definitions

**Table 1. Ball Descriptions**

| Symbol | Type | Name and function |
|---|---|---|
| CA[9:0] | Input | Command/address inputs : Provide the command and address inputs according to the command truth table. |
| CK, CK# | Input | Clock: CK and CK# are differential clock inputs. All CA inputs are sampled on both rising and falling edges of CK. CS and CKE inputs are sampled at the rising edge of CK. AC timings are referenced to clock. |
| CKE[1:0] | Input | Clock enable : CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions.<br>CKE is considered part of the command code. CKE is sampled at the rising edge of CK. |
| CS[1:0]# | Input | Chip select : CS# is considered part of the command code and is sampled at the rising edge of CK. |
| DM[3:0] | Input | Input data mask : DM is an input mask signal for write data. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. DM[3:0] is DM for each of the four data bytes, respectively. |
| DQ[31:0] | I/O | Data input/output : Bidirectional data bus. |
| DQS[3:0], DQS[3:0]# | I/O | Data strobe : The data strobe is bidirectional (used for read and write data) and complementary (DQS and DQS#). It is edge-aligned output with read data and centered input with write data.<br>DQS[3:0]/DQS[3:0]# is DQS for each of the four data bytes, respectively. |
| VDDQ | Supply | DQ power supply : Isolated on the die for improved noise immunity. |
| VSSQ | Supply | DQ ground : Isolated on the die for improved noise immunity. |
| VDDCA | Supply | Command/address power supply: Command/address power supply. |
| VSSCA | Supply | Command/address ground: Isolated on the die for improved noise immunity. |
| VDD1 | Supply | Core power : Supply 1. |
| VDD2 | Supply | Core power : Supply 2. |
| VSS | Supply | Common ground |
| VREFCA, VREFDQ | Supply | Reference voltage : VREFCA is reference for command/address input buffers, VREFDQ is reference for DQ input buffers. |
| ZQ | Reference | External impedance (240 ohm) : This signal is used to calibrate the device out-put impedance for S4 devices. For S2 devices, ZQ should be tied to VDDCA. |
| DNU | – | Do not use : Must be grounded or left floating. |
| NC | – | No connect : Not internally connected. |
| (NC) | – | No connect : Balls indicated as (NC) are no connects, however, they could be connected tighter internally. |

# 2.0. Absolute Maximum Ratings

**Table 2. Absolute Maximum Ratings**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| $V_{DD1}$ supply voltage relative to $V_{SS}$ | $V_{DD1}$ | –0.4 | +2.3 | V | 1 |
| $V_{DD2}$ supply voltage relative to $V_{SS}$ | $V_{DD2}$ (1.2V) | –0.4 | +1.6 | V | 1 |
| $V_{DDCA}$ supply voltage relative to $V_{SSCA}$ | $V_{DDCA}$ | –0.4 | +1.6 | V | 1, 2 |
| $V_{DDQ}$ supply voltage relative to $V_{SSQ}$ | $V_{DDQ}$ | –0.4 | +1.6 | V | 1, 3 |
| Voltage on any ball relative to $V_{SS}$ | $V_{IN}$, $V_{OUT}$ | –0.4 | +1.6 | V | |
| Storage temperature | $T_{STG}$ | –55 | +125 | °C | 4 |

Notes:
1. See 1. Voltage Ramp under Power-Up
2. $V_{REFCA}$ 0.6 ≤ $V_{DDCA}$; however, $V_{REFCA}$ may be ≥ $V_{DDCA}$ provided that $V_{REFCA}$ ≤ 300mV.
3. $V_{REFDQ}$ 0.6 ≤ $V_{DDQ}$; however, $V_{REFDQ}$ may be ≥ $V_{DDQ}$ provided that $V_{REFDQ}$ ≤ 300mV.
4. Storage temperature is the case surface temperature on the center/top side of the device. For measurement conditions, refer to the JESD51-2 standard.

Caution: Stressing greater than those listed above Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of these specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect device reliability.

# 3.0 DC and AC Parameters

Warning: Operation beyond the Operating Conditions is not recommended, and extended exposure beyond the Operating Conditions may affect device reliability.

The parameter in the DC and AC characteristics tables are derived from tests performed under conditions in Table 3.

**Table 3. Operating Measurement Conditions**

| Symbol | LPDDR2-S4B | | | Power Supply | Unit |
|---|---|---|---|---|---|
| | Min | Typ | Max | | |
| $V_{DD1}$[1] | 1.70 | 1.80 | 1.95 | Core power 1 | V |
| $V_{DD2}$ | 1.14 | 1.20 | 1.30 | Core power 2 | V |
| $V_{DDCA}$ | 1.14 | 1.20 | 1.30 | Input buffer power | V |
| $V_{DDQ}$ | 1.14 | 1.20 | 1.30 | I/O buffer power | V |

Note: 1. $V_{DD1}$ uses significantly less power than $V_{DD2}$.

## 3.1 DC Characteristics

### Table 4. IDD Specification Parameters and Operating Conditions

TC = -30°C to +85°C, VDD1 = 1.70V to 1.95V, VDD2, VDDQ, VDDCA = 1.14V to 1.30V

| Symbol | Power Supply | 800 max. | Unit | Parameter/Condition |
|---|---|---|---|---|
| IDD0_1 | VDD1 | 15 | mA | **Operating one bank active-precharge current (SDRAM)**: tCK = tCKmin; tRC = tRCmin; CKE is HIGH; CS# is HIGH between valid commands; CA bus in- puts are switching; Data bus inputs are stable. |
| IDD0_2 | VDD2 | 70 | mA | |
| IDD0_IN | VDDCA+VDDQ | 6 | mA | |
| IDD2P_1 | VDD1 | 600 | µA | **Idle power-down standby current: tCK = tCKmin**; CKE is LOW; CS# is HIGH; All banks are idle; CA bus inputs are switching; Data bus inputs are stable |
| IDD2P_2 | VDD2 | 800 | µA | |
| IDD2P_IN | VDDCA+VDDQ | 50 | µA | |
| IDD2PS_1 | VDD1 | 600 | µA | **Idle power-down standby current with clock stop**: CK = LOW, CK# = HIGH; CKE is LOW; CS# is HIGH; All banks are idle; CA bus inputs are stable; Data bus inputs are stable |
| IDD2PS_2 | VDD2 | 800 | µA | |
| IDD2PS_IN | VDDCA+VDDQ | 50 | µA | |
| IDD2N_1 | VDD1 | 2 | mA | **Idle non-power-down standby current: tCK = tCKmin**; CKE is HIGH; CS# is HIGH; All banks are idle; CA bus inputs are switching; Data bus inputs are stable |
| IDD2N_2 | VDD2 | 30 | mA | |
| IDD2N_IN | VDDCA+VDDQ | 6 | mA | |
| IDD2NS_1 | VDD1 | 1.7 | mA | **Idle non-power-down standby current with clock stopped:** CK = LOW; CK# = HIGH; CKE is HIGH; CS# is HIGH; All banks are idle; CA bus inputs are stable; Data bus inputs are stable |
| IDD2NS_2 | VDD2 | 27 | mA | |
| IDD2NS_IN | VDDCA+VDDQ | 6 | mA | |
| IDD3P_1 | VDD1 | 1200 | µA | **Active power-down standby current**: tCK = tCKmin; CKE is LOW; CS# is HIGH; One bank is active; CA bus inputs are switching; Data bus inputs are stable |
| IDD3P_2 | VDD2 | 8 | mA | |
| IDD3P_IN | VDDCA+VDDQ | 150 | µA | |
| IDD3PS_1 | VDD1 | 1200 | µA | **Active power-down standby current with clock stop**: CK = LOW, CK# = HIGH; CKE is LOW; CS# is HIGH; One bank is active; CA bus inputs are stable; Data bus inputs are stable |
| IDD3PS_2 | VDD2 | 8 | mA | |
| IDD3PS_IN | VDDCA+VDDQ | 150 | µA | |
| IDD3N_1 | VDD1 | 2.5 | mA | **Active non-power-down standby current:** tCK = tCKmin; CKE is HIGH; CS# is HIGH; One bank is active; CA bus inputs are switching; Data bus inputs are stable |
| IDD3N_2 | VDD2 | 30 | mA | |
| IDD3N_IN | VDDCA+VDDQ | 6 | mA | |
| IDD3NS_1 | VDD1 | 2 | mA | **Active non-power-down standby current with clock stopped:** CK = LOW, CK# = HIGH CKE is HIGH; CS# is HIGH; One bank is active; CA bus inputs are stable; Data bus inputs are stable |
| IDD3NS_2 | VDD2 | 27 | mA | |
| IDD3NS_IN | VDDCA+VDDQ | 6 | mA | |
| IDD4R_1 | VDD1 | 3 | mA | **Operating burst READ current:** tCK = tCKmin; CS# is HIGH between valid commands; One bank is active; BL = 4; RL = RL (MIN); CA bus inputs are switching; 50% data change each burst transfer |
| IDD4R_2 | VDD2 | 194 | mA | |
| IDD4R, IN | VDDCA | 6 | mA | |

## IDD Specification Parameters and Operating Conditions (cont'd)

| Symbol | Power Supply | 800 max. | Unit | Parameter/Condition |
|---|---|---|---|---|
| IDD4W_1 | VDD1 | 10 | mA | **Operating burst WRITE current:** tCK = tCKmin; CS# is HIGH between valid commands; One bank is active; BL = 4; WL = WLmin; CA bus inputs are switching; 50% data change each burst transfer |
| IDD4W_2 | VDD2 | 185 | mA | |
| IDD4W_IN | VDDCA+VDDQ | 25 | mA | |
| IDD5_1 | VDD1 | 40 | mA | **All-bank REFRESH burst current:** tCK = tCKmin; CKE is HIGH between valid commands; tRC = tRFCabmin; Burst refresh; CA bus inputs are switching; Data bus inputs are stable |
| IDD5_2 | VDD2 | 150 | mA | |
| IDD5_IN | VDDCA+VDDQ | 6 | mA | |
| IDD5AB_1 | VDD1 | 5 | mA | **All-bank REFRESH average current (–30˚C to +85˚C):** tCK = tCKmin; CKE is HIGH between valid commands; tRC = tREFI; CA bus inputs are switching; Data bus inputs are stable |
| IDD5AB_2 | VDD2 | 50 | mA | |
| IDD5AB_IN | VDDCA+VDDQ | 8 | mA | |
| IDD5PB_1 | VDD1 | 5 | mA | **Per-bank REFRESH average current (–30˚C to +85˚C):** tCK = tCKmin; CKE is HIGH between valid commands; tRC = tREFI/8; CA bus inputs are switching; Data bus inputs are stable |
| IDD5PB_2 | VDD2 | 50 | mA | |
| IDD5PB_IN | VDDCA+VDDQ | 8 | mA | |
| IDD6_1 | VDD1 | 1000 | µA | **Self refresh current (–30˚C to +85˚C):** CK = LOW, CK# = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable; Maximum 1x self refresh rate |
| IDD6_2 | VDD2 | 3200 | µA | |
| IDD6_IN | VDDCA+VDDQ | 50 | µA | |
| IDD8_1 | VDD1 | 25 | µA | **Deep power-down current:** CK = LOW, CK# = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable |
| IDD8_2 | VDD2 | 100 | µA | |
| IDD8_IN | VDDCA+VDDQ | 100 | µA | |

## Table 5. DD6 Full and Partial Array Self-Refresh Current

TC = -30°C to +85°C, VDD1 = 1.70V to 1.95V, VDD2, VDDQ, VDDCA = 1.14V to 1.30V

| Parameter | | Symbol | max. | Unit | Note |
|---|---|---|---|---|---|
| Self-Refresh Current<br>-30°C ≤ TC ≤ +85°C | Full Array | IDD6_1 | 1000 | µA | LPDDR2-S4 SDRAM devices support both bank masking and segment masking. IDD6 PASR current are measured using bank masking only |
| | | IDD6_2 | 3.2 | mA | |
| | | IDD6_IN | 50 | µA | |
| | 1/2 Array | IDD6_1 | 950 | µA | |
| | | IDD6_2 | 2700 | µA | |
| | | IDD6_IN | 50 | µA | |
| | 1/4 Array | IDD6_1 | 900 | µA | |
| | | IDD6_2 | 2400 | µA | |
| | | IDD6_IN | 50 | µA | |
| | 1/8 Array | IDD6_1 | 850 | µA | |
| | | IDD6_2 | 2000 | µA | |
| | | IDD6_IN | 50 | µA | |

## Table 6. Input Leakage current

| Parameter/Condition | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| **Input leakage current:** For CA, CKE, CS#, CK, CK#; Any input 0V ≤ $V_{IN}$ ≤ $V_{DDCA}$; (All other pins not under test = 0V) | $I_L$ | –2 | 2 | µA | 1 |
| **$V_{REF}$ supply leakage current:** $V_{REFDQ}$ = $V_{DDQ}$/2, or $V_{REFCA}$ = $V_{DDCA}$/2; (All other pins not under test = 0V) | $I_{VREF}$ | –1 | 1 | µA | 2 |

Notes:
1. Although DM is for input only, the DM leakage must match the DQ and DQS/DQS# output leakage specification.
2. The minimum limit requirement is for testing purposes. The leakage current on $V_{REFCA}$ and $V_{REFDQ}$ pins should be minimal.

## 3.2 AC Characteristics

### Table 7. AC Characteristics

Note 1-2 apply to all parameters and conditions. AC timing parameters must satisfy the $^{t}$CK minimum conditions (in multiples of $^{t}$CK) as well the timing specifications when values for both are indicated

| Parameter | Symbol | min. max. | min. $^{t}$CK | 800 | Unit | Notes |
|---|---|---|---|---|---|---|
| Max. Frequency | | | — | 400 | MHz | |
| **Clock Timing** | | | | | | |
| Average Clock Period | $^{t}$CK(avg) | min. | — | 2.5 | ns | |
| | | max. | — | 100 | ns | |
| Average high pulse width | $^{t}$CH(avg) | min. | — | 0.45 | tCK(avg) | |
| | | max. | — | 0.55 | | |
| Average low pulse width | $^{t}$CL(avg) | min. | — | 0.45 | tCK(avg) | |
| | | max. | — | 0.55 | | |
| Absolute Clock Period | tCK(abs) | min. | — | tCK(avg)(min.) + tJIT(per)(min.) | ps | |
| Absolute clock HIGH pulse width (with allowed jitter) | tCH(abs), allowed | min. | — | 0.43 | tCK(avg) | |
| | | max. | — | 0.57 | | |
| Absolute clock LOW pulse width (with allowed jitter) | tCL(abs), allowed | min. | — | 0.43 | tCK(avg) | |
| | | max. | — | 0.57 | | |
| Clock Period Jitter (with allowed jitter) | tJIT(per), allowed | min. | — | -100 | ps | |
| | | max. | — | 100 | | |
| Maximum Clock Jitter between two consecutive clock cycles (with allowed jitter) | tJIT(cc), allowed | max. | — | 200 | ps | |
| Duty cycle Jitter (with allowed jitter) | tJIT(duty), allowed | min. | — | min((tCH(abs),min -tCH(avg),min), (tCL(abs),min - tCL(avg),min)) × tCK(avg) | ps | |
| | | max. | — | max((tCH(abs),max -tCH(avg),max), (tCL(abs),max -tCL(avg),max)) × tCK(avg) | | |
| Cumulative error across 2 cycles | tERR(2per), allowed | min. | — | -147 | ps | |
| | | max. | — | 147 | | |
| Cumulative error across 3 cycles | tERR(3per), allowed | min. | — | -175 | ps | |
| | | max. | — | 175 | | |
| Cumulative error across 4 cycles | tERR(4per), allowed | min. | — | -194 | ps | |
| | | max. | — | 194 | | |
| Cumulative error across 5 cycles | tERR(5per), allowed | min. | — | -209 | ps | |
| | | max. | — | 209 | | |
| Cumulative error across 6 cycles | tERR(6per), allowed | min. | — | -222 | ps | |
| | | max. | — | 222 | | |
| Cumulative error across 7 cycles | tERR(7per), allowed | min. | — | -232 | ps | |
| | | max. | — | 232 | | |

| Parameter | Symbol | min. max. | min. tCK | 800 | Unit | Notes |
|---|---|---|---|---|---|---|
| Cumulative error across 8 cycles | tERR(8per), allowed | min. | — | -241 | ps | |
| | | max. | — | 241 | | |
| Cumulative error across 9 cycles | tERR(9per), allowed | min. | — | -249 | ps | |
| | | max. | — | 249 | | |
| Cumulative error across 10 cycles | tERR(10per), allowed | min. | — | -257 | ps | |
| | | max. | — | 257 | | |
| Cumulative error across 11 cycles | tERR(11per), allowed | min. | — | -263 | ps | |
| | | max. | — | 263 | | |
| Cumulative error across 12 cycles | tERR(12per), allowed | min. | — | -269 | ps | |
| | | max. | — | 269 | | |
| Cumulative error across n = 13, 14 . . . 49, 50 cycles | tERR(nper), allowed | min. | — | tERR(nper),allowed,min. = (1 + 0.68ln(n)) × tJIT(per),allowed,min. | ps | |
| | | max. | — | tERR(nper),allowed,max. = (1 + 0.68ln(n)) × tJIT(per),allowed,max. | | |
| **ZQ Calibration Parameters** | | | | | | |
| Initialization calibration time | tZQINIT | min. | — | 1 | µs | |
| Long calibration time | tZQCL | min | 6 | 360 | ns | |
| Short calibration time | tZQCS | min | 6 | 90 | ns | |
| Calibration RESET time | tZQRESET | min | 3 | 50 | ns | |
| **READ Parameters[3]** | | | | | | |
| DQS output access time from CK/CK# | tDQSCK | min. | — | 2500 | ps | |
| | | max. | — | 5500 | | |
| DQSCK Delta Short | tDQSCKDS | max. | — | 450 | ps | 4 |
| DQSCK Delta Medium | tDQSCKDM | max. | — | 900 | ps | 5 |
| DQSCK Delta Long | tDQSCKDL | max. | — | 1200 | ps | 6 |
| DQS – DQ skew | tDQSQ | max. | — | 240 | ps | |
| Data hold skew factor | tQHS | max. | — | 280 | ps | |
| DQS Output High Pulse Width | tQSH | min. | — | tCH(abs) - 0.05 | tCK(avg) | |
| DQS Output Low Pulse Width | tQSL | min. | — | tCL(abs) - 0.05 | tCK(avg) | |
| Data Half Period | tQHP | min. | — | min(tQSH, tQSL) | tCK(avg) | |
| DQ / DQS output hold time from DQS | tQH | min. | — | tQHP - tQHS | ps | |
| Read preamble | tRPRE | min. | — | 0.9 | tCK(avg) | 7 |
| Read postamble | tRPST | min. | — | tCL(abs) - 0.05 | tCK(avg) | 8 |
| DQS low-Z from clock | tLZ(DQS) | min. | — | tDQSCK(min.) - 300 | ps | |
| DQ low-Z from clock | tLZ(DQ) | min. | — | tDQSCK(min.) - (1.4 × tQHS(max.)) | ps | |
| DQS high-Z from clock | tHZ(DQS) | max. | — | tDQSCK(max.) - 100 | ps | |
| DQ high-Z from clock | tHZ(DQ) | max. | — | tDQSCK(max.) + (1.4 × tDQSQ(max.)) | ps | |

| Parameter | Symbol | min. max. | min. tCK | 800 | Unit | Notes |
|---|---|---|---|---|---|---|
| **Write Parameters**[3] | | | | | | |
| DQ and DM input hold time (VREF based) | tDH | min. | — | 270 | ps | |
| DQ and DM input setup time (VREF based) | tDS | min. | — | 270 | ps | |
| DQ and DM input pulse width | tDIPW | min. | — | 0.35 | tCK(avg) | |
| Write command to 1st DQS latching transition | tDQSS | min. | — | 0.75 | tCK(avg) | |
| | | max. | — | 1.25 | | |
| DQS input high-level width | tDQSH | min. | — | 0.4 | tCK(avg) | |
| DQS input low-level width | tDQSL | min. | — | 0.4 | tCK(avg) | |
| DQS falling edge to CK setup time | tDSS | min. | — | 0.2 | tCK(avg) | |
| DQS falling edge hold time from CK | tDSH | min. | — | 0.2 | tCK(avg) | |
| Write postamble | tWPST | min. | — | 0.4 | tCK(avg) | |
| Write preamble | tWPRE | min. | — | 0.35 | tCK(avg) | |
| **CKE Input Parameters** | | | | | | |
| CKE min. pulse width (high and low pulse width) | tCKE | min. | 3 | 3 | tCK(avg) | |
| CKE input setup time | tISCKE*2 | min. | — | 0.25 | tCK(avg) | 9 |
| CKE input hold time | tIHCKE*3 | min. | — | 0.25 | tCK(avg) | 10 |
| **Command Address Input Parameters**[3] | | | | | | |
| Address and control input setup time | tIS | min. | — | 290 | ps | 11 |
| Address and control input hold time | tIH | min. | — | 290 | ps | 11 |
| Address and control input pulse width | tIPW | min. | — | 0.4 | tCK(avg) | |
| **Boot Parameters (10 MHz – 55 MHz)**[12, 13, 14] | | | | | | |
| Clock Cycle Time | tCKb | max. | — | 100 | ns | |
| | | min. | — | 18 | | |
| CKE Input Setup Time | tISCKEb | min. | — | 2.5 | ns | |
| CKE Input Hold Time | tIHCKEb | min. | — | 2.5 | ns | |
| Address & Control Input Setup Time | tISb | min. | — | 1150 | ps | |
| Address & Control Input Hold Time | tIHb | min. | — | 1150 | ps | |
| DQS Output Data Access Time from CK, /CK | tDQSCKb | min. | — | 2.0 | ns | |
| | | max. | — | 10.0 | | |
| Data Strobe Edge to Ouput Data Edge tDQSQb | tDQSQb | max. | — | 1.2 | ns | |
| Data Hold Skew Factor | tQHSb | max. | — | 1.2 | ns | |
| **Mode Register Parameters** | | | | | | |
| Mode Register Write command period | tMRW | min. | 3 | 3 | tCK(avg) | |
| Mode Register Read command period | tMRR | min. | 2 | 2 | tCK(avg) | |

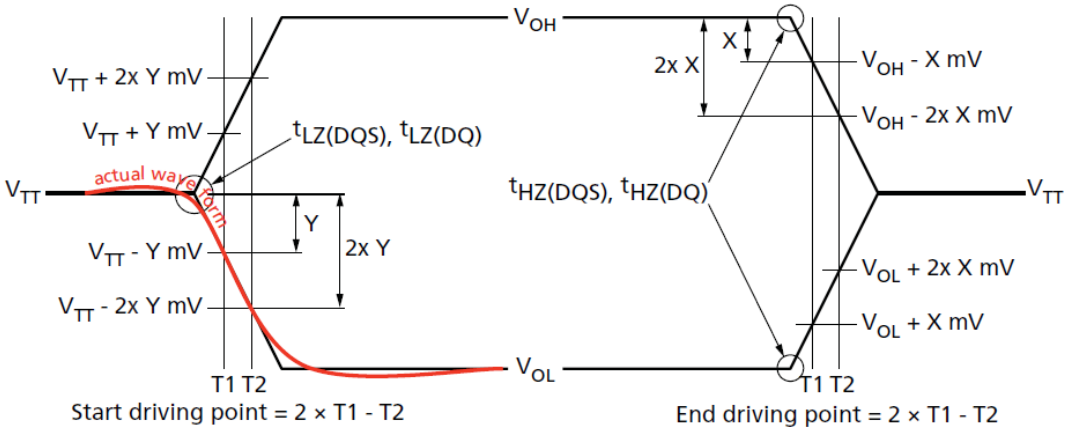
| Parameter | Symbol | min. max. | min. tCK*9 | 800 | Unit | Notes |
|---|---|---|---|---|---|---|
| **Core Parameters**[15] | | | | | | |
| Read Latency | RL | min. | 3 | 6 | tCK(avg) | |
| Write Latency | WL | min. | 1 | 3 | tCK(avg) | |
| ACTIVE to ACTIVE command period | tRC | min. | — | tRAS + tRPab (with all-bank Precharge) tRAS + tRPpb(with per-bank Precharge) | ns | 17 |
| CKE min. pulse width during Self-Refresh (low pulse width during Self-Refresh) | tCKESR | min. | 3 | 15 | ns | |
| Self-refresh exit to next valid command delay | tXSR | min. | 2 | tRFCab + 10 | ns | |
| Exit power down to next valid command delay | tXP | min. | 2 | 7.5 | ns | |
| CAS to CAS delay | tCCD | min. | 2 | 2 | tCK(avg) | |
| Internal Read to Precharge command delay | tRTP | min. | 2 | 7.5 | ns | |
| RAS to CAS Delay | tRCD | Fast. | 3 | 15 | ns | |
| | | TYP | 3 | 18 | | |
| Row Precharge Time (single bank) | tRPpb | Fast. | 3 | 15 | ns | |
| | | TYP | 3 | 18 | | |
| Row Precharge Time (all banks) | tRPab | Fast. | 3 | 18 | ns | |
| | | TYP | 3 | 21 | | |
| Row Active Time | tRAS | min. | 3 | 42 | ns | |
| | | max. | — | 70 | µs | |
| Write Recovery Time | tWR | min. | 3 | 15 | ns | |
| Internal Write to Read Command Delay | tWTR | min. | 2 | 7.5 | ns | |
| Active bank A to Active bank B | tRRD | min. | 2 | 10 | ns | |
| Four Bank Activate Window | tFAW | min. | 8 | 50 | ns | |
| Minimum Deep Power Down Time | tDPD | min. | — | 500 | µs | |
| **Temperature Derating**[16] | | | | | | |
| tDQSCK derating | tDQSCK (derated) | max. | — | 6000 | ps | |
| Core timing temperature derating | tRCD (derated) | min. | — | tRCD + 1.875 | ns | |
| | tRC (derated) | min | — | tRC + 1.875 | ns | |
| | tRAS (derated) | min | — | tRAS + 1.875 | ns | |
| | tRP (derated) | min. | — | tRP + 1.875 | ns | |
| | tRRD (derated) | min. | — | tRRD + 1.875 | ns | |

Note:

1. Frequency values are for reference only. Clock cycle time (tCK) is used to determine device capabilities.
2. All AC timings assume an input slew rate of 1 V/ns.
3. READ, WRITE, and input setup and hold values are referenced to VREF.
4. tDQSCKDS is the absolute value of the difference between any two tDQSCK measurements (in a byte lane) within a contiguous sequence of bursts in a 160ns rolling window. tDQSCKDS is not tested and is guaranteed by design. Temperature drift in the system is <10˚ C/s. Values do not include clock jitter.
5. tDQSCKDM is the absolute value of the difference between any two tDQSCK measurements (in a byte lane) within a 1.6µ s rolling window. tDQSCKDM is not tested and is guaranteed by design. Temperature drift in the system is <10˚ C/s. Values do not include clock jitter.

6. tDQSCKDL is the absolute value of the difference between any two tDQSCK measurements (in a byte lane) within a 32ms rolling window. tDQSCKDL is not tested and is guaranteed by design. Temperature drift in the system is <10˚ C/s. Values do not include clock jitter. For LOW-to-HIGH and HIGH-to-LOW transitions, the timing reference is at the point when the signal crosses the transition threshold (VTT). tHZ and tLZ transitions occur in the same access time (with respect to clock) as valid data transitions. These parameters are not referenced to a specific voltage level but to the time when the device output is no longer driving (for tRPST, tHZ(DQS) and tHZ(DQ)), or begins driving (for tRPRE, tLZ(DQS), tLZ(DQ)). The figure below shows a method to calculate the point when the device is no longer driving tHZ(DQS) and tHZ(DQ) or begins driving tLZ(DQS) and tLZ(DQ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as single-ended. The timing parameters tRPRE and tRPST are determined from the differential signal DQS/DQS#.

**Output Transition Timing**




7. Measured from the point when DQS/DQS# begins driving the signal, to the point when DQS/DQS# begins driving the first rising strobe edge.

8. Measured from the last falling strobe edge of DQS/DQS# to the point when DQS/DQS# finishes driving the signal.

9. CKE input setup time is measured from CKE reaching a HIGH/LOW voltage level to CK/CK# crossing.

10. CKE input hold time is measured from CK/CK# crossing to CKE reaching a HIGH/LOW voltage level.

11. Input setup/hold time for signal (CA[9:0], CS#).

12. To ensure device operation before the device is configured, a number of AC boot timing parameters are defined in this table. The letter b is appended to the boot parameter symbols (for example, tCK during boot is tCKb).

13. Mobile LPDDR2 devices set some mode register default values upon receiving a RESET (MRW) command, as specified in Mode Register Definition.

14. The output skew parameters are measured with default output impedance settings using the reference load.

15. The minimum tCK column applies only when tCK is greater than 6ns.

16. Timing derating applies for operation at 85˚ C to 105˚ C when the requirement to derate is indicated by mode register 4 op-code (see the MR4 Device Temperature (MA[7:0] = 04h) table).

17. DRAM devices should be evenly addressed when being accessed. Disproportionate accesses to a particular row address may result in reduction of the product lifetime.

# 4.0 Capacitance

**Table 8. LP-DDR2 Capacitance**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input Capacitance (CK, CK#) | $C_{CK}$ | 1.0 | 2.0 | pF | 2,3 |
| Input Capacitance delta (CK, CK#) | $C_{DCK}$ | 0 | 0.2 | pF | 2,3,4 |
| Input Capacitance all other input-only pins | $C_{I}$ | 1.0 | 2 | pF | 2,3,5 |
| Input Capacitance delta,all other input-only pins | $C_{DI}$ | -0.40 | +4.0 | pF | 2,3,6 |
| input/output capacitance DQ,DM,DQS,DQS# | $C_{IO}$ | 1.25 | 2.5 | pF | 2,3,7,8 |
| input/output capacitance delta,DQS,DQS# | $C_{DDQS}$ | 0 | 0.25 | pF | 2,3,8,9 |
| input/output capacitance delta,DQ,DM | $C_{DIO}$ | -0.5 | +0.5 | pF | 2,3,8,10 |
| Input/output capacitance ZQ | $C_{ZQ}$ | 0 | 2.5 | pF | 2,3,11 |

Notes:

1.TC – 40° C to +105° C; VDDQ = 1.14– 1.3V; VDDCA = 1.14– 1.3V; VDD1 = 1.7– 1.95V; VDD2 = 1.28– 1.42V; apply to all parameter and conditions.

2. This parameter applies to die devices only (does not include package capacitance).

3. This parameter is not subject to production testing. It is verified by design and characterization. The capacitance is measured according to JEP147 (procedure for measuring input capacitance using a vector network analyzer), with VDD1, VDD2, VDDQ, VSS, VSSCA,and VSSQ applied; all other pins are left floating.

4. Absolute value of CCK - CCK#.

5. CI applies to CS#, CKE, and CA[9:0].

6. CDI = CI - 0.5 × (CCK + CCK#).

7. DM loading matches DQ and DQS.

8. MR3 I/O configuration drive strength OP[3:0] = 0001b (34.3 ohm typical).

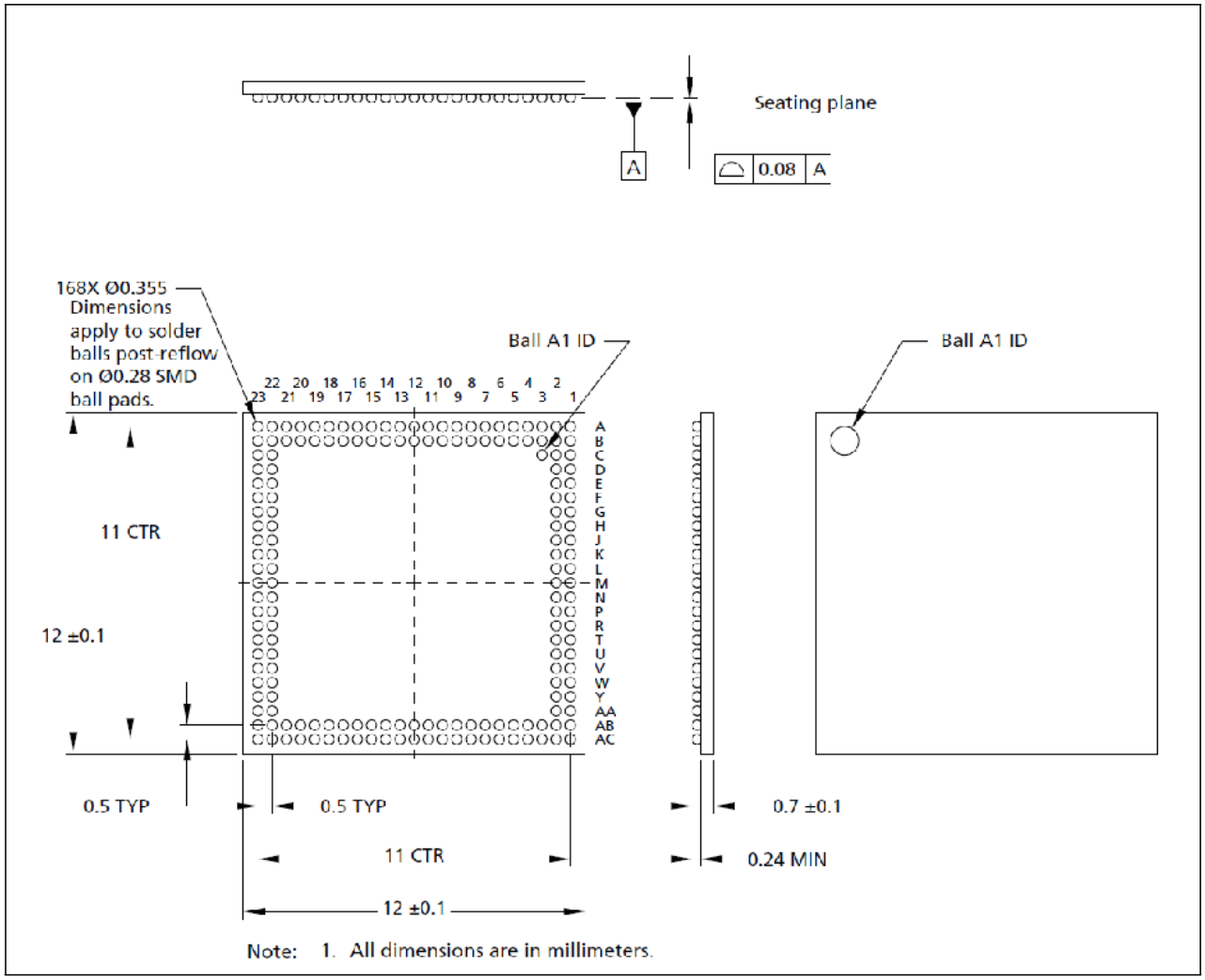
9. Absolute value of CDQS and CDQS#.

10. CDIO = CIO - 0.5 × (CDQS + CDQS#) in byte-lane.

11. Maximum external load capacitance on ZQ pin: 5pF.

# 5.0 Mechanical Specification

Figure 3. Mechanical Specifications for 168-ball Package



## 5.1 Ordering Information

| Part No. | Density | LPDDR2 Voltage | Package(max.) |
|---|---|---|---|
| KPN005SS-ZBw2 | 512MB LP-DDR2 | $V_{DD2}$ = 1.14–1.30V $V_{DDCA}$/$V_{DDQ}$ = 1.14–1.30V $V_{DD1}$ = 1.70–1.95V | 12x12x0.8mm |

## Revision History

| Revision No. | Contents |
|---|---|
| V0.10 | Initial release |
| V0.20 | Modify the data rate from 1066 to 800 |