

8Gb DDP LPDDR3 SDRAM

178FBGA, 11x11.5, 2/CS, 2CKE
128M x32 (16M x32 x 8banks) + 128M x32 (16M x32 x 8banks)

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datasheet

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Revision History

| <u>Revision No.</u> | <u>History</u> | <u>Draft Date</u> | <u>Remark</u> | <u>Editor</u> |
|---------------------|--|-------------------|---------------|---------------|
| 0.0 | - First version for target specification. - K4E4E324EE-EGCF(CE)_Ver 0.0 | 27th Jan, 2014 | Target | J.Y.Bae |
| 0.5 | - Revise DC values. | 6th Mar, 2014 | Preliminary | J.Y.Bae |
| 1.0 | - Final datasheet. - Update IDD Spec values. 1. Add 1866Mbps values. 2. Update 1600Mbps VDD2. - IDD0 : 56.5 -> 51.5 [mA] - IDD2N : 19.5 -> 13.5 [mA] - IDD2NS : 13.5 -> 11.5 [mA] - IDD3N : 22.5 -> 16.5 [mA] - IDD3NS : 16.5 -> 14.5 [mA] - IDD5AB : 21.5 -> 19.5 [mA] - IDD5PB : 23.5 -> 21.5 [mA] | 24th Apr, 2014 | Final | J.Y.Bae |

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1.0 COMPARISION BETWEEN LPDDR2 AND LPDDR3

| | Items | LPDDR2 | LPDDR3 |
|--|------------------------------------|---|----------------------------|
| Feature | CLK scheme | Differential (CLK/CLKB) | ← |
| | Data scheme | DDR Single-ended, Bi-Directional | ← |
| | DQS scheme | Differential (DQS/DQSB), Bi-Directional | ← |
| | ADD / CMD scheme | DDR | ← |
| | State Diagram | As is | Refer to the Datasheet |
| | Command Truth Table | As is | No support BST |
| | State for bank n to Bank n/m | As is | No support BST / Interrupt |
| | Data mask Truth Table | As is | ← |
| | I/O Interface | HSUL_12 | ← |
| | Burst Length | 4(Default), 8, 16 | 8 |
| | Burst Type | Sequential, Interleave | Sequential |
| | No Wrap | Support (BL4) | No support |
| | # of Bank | 8 | 8 |
| | Organization | x16/x32 | ← |
| | Data Mask | Support (Write) | ← |
| | Refresh mode | All Bank Refresh / Per Bank Refresh / Self Refresh | ← |
| Addressing(x32) | Row | Refer to the Datasheet | Refer to the Datasheet |
| | Column | | |
| | Bank | | |
| | Refresh Requirements | | |
| AC Parameter | Speed bin [Mbps] | 667/800/1066 | 1600/1866 |
| | Read/Write latency | Refer to the Datasheet | Refer to the Datasheet |
| | Core Parameters | | |
| | IO Parameters | | |
| | CA / CS_n / Setup / Hold / Deratin | | |
| | Data Setup / Hold / Deratin | | |
| Special Function | PASR | Support | ← |
| | TCSR | Support | ← |
| | Deep Power Down | Support | No Support |
| | Configurable D/S | Support | ← |
| | ZQ Calibration | Support | ← |
| | DQ Calibration | Support | ← ¹⁾ |
| | CA Calibration | N/A | Support |
| | Write Leveling | N/A | Support |
| Power Supply | VDD1 [V] | 1.70 ~ 1.95 | ← |
| | VDD2 [V] | 1.14 ~ 1.30 | ← |
| | VDDQ [V] | 1.14 ~ 1.30 | ← |
| | VDDCA [V] | 1.14 ~ 1.30 | ← |
| IDD Specification Parameters and Test Conditions | IDD Measurement Conditions | As is | ← |
| | IDD Specification | As is | ← |
| Temperature | General [°C] | -25 ~ 85 | ← |
| | Extended [°C] | -25 ~ 105 | ← |

| | | Items | LPDDR2 | LPDDR3 | |
|--|---|-------------------------------------|--|---|------------|
| Mode Register Set | | General | As is | ← | |
| | | Modified | Support | MR0 DI ²⁾ | |
| | | | Support | MR1 BL/WC/nWR ²⁾ | |
| | | | Support | MR2 RL & WL, nWRE ²⁾ | |
| | | | Support | MR3 DS ²⁾ | |
| | | | Support | MR4 Refresh Rate (0.5*tREFI) ²⁾ | |
| | | | Support | MR8 I/O width, Type ²⁾ | |
| | | | Adding | N/A | MR41/42/48 |
| | | N/A | | MR2 OP7(Write Leveling) | |
| RONpu/RONpd Characteristics | | w/ ZQ Calibration | As is | ← | |
| | | w/o ZQ Calibration | As is | ← | |
| | | Temperature and Voltage Sensitivity | As is | ← | |
| | | RZQI-V Curve | As is | ← | |
| Input/Output Capacitance ³⁾ | | | As is | ← | |
| Absolute maximum DC ratings | | VDD1 [V] | -0.4 ~ 2.3 | ← | |
| | | VDD2 [V] | -0.4 ~ 1.6 | ← | |
| | | VDDQ [V] | -0.4 ~ 1.6 | ← | |
| | | VDDCA [V] | -0.4 ~ 1.6 | ← | |
| | | VIN/VOUT [V] | -0.4 ~ 1.6 | ← | |
| | | Tstg [°C] | -55 ~ 125 | ← | |
| | | Input leakage | As is | ← | |
| Input/Output Operating condition | AC/DC Logic Input Levels for Single-ended Signals | CA and CS_n pins | AC : VREF +/- 0.22V DC : VREF +/- 0.13V | AC : VREF ± 0.150V / ±0.135V (1600/1866) DC : VREF ± 0.10V / ± 0.10V (1600/1866) | |
| | | CKE pin | 0.2*VDDCA ~ 0.8*VDDCA | ← | |
| | | DQ pins | AC : VREF +/- 0.22V DC : VREF +/- 0.13V | AC : VREF ± 0.15V/ ±0.135V(1600/1866) DC : VREF ± 0.10V/0.10V (1600/1866) | |
| | | VREF_CA/DQ tolerance | 0.49*VDDQ ~ 0.51*VDDQ | ← | |
| | AC/DC Logic Input Levels for Differential | VIHdiff/VILdiff (AC/DC) tDVAC | As is | ← | |
| | | VSEH/VSEL(AC) | As is | ← | |
| | Differential Input Cross Point Voltage | VIXCA/VIXDQ | As is | ← | |
| | Slew Rate definitions for Differential | VILdiff /VIHdiff (Max/Min) | As is | ← | |
| | AC/DC Output levels for Differential | VOHdiff / VOLdiff (AC) | As is | ← | |
| | | IOZ | As is | ← | |
| | | MMPUPD | As is | ← | |
| | AC/DC Output levels for Differential | VOHdiff / VOLdiff (AC) | As is | ← | |
| | Signal ended output Slew Rate | VOH/VOL(AC/DC) | As is | ← | |
| | | SROse | As is | ← | |
| | Differential Output Slew Rate | VOHdiff/VOLdiff(AC) | As is | ← | |
| | | SRQdiff | As is | ← | |
| | Overshoot / Undershoot | Maximum Amplitude | As is | ← | |
| | | Maximum Area | As is | VDD/VSS : 0.1 [V-ns] | |
| | HSUL_12 Driver Output Timing | | | As is | ← |

NOTE :

1) DQ out data are same in a byte.

2) These items are modified from LPDDR2 specification. Please refer to Mode Register Definition.

3) The parameter applies to both die and package.

LPDDR3 SDRAM SPECIFICATION

8G DDP = 128M x 32(16M x 32 x 8 banks) + 128M x 32(16M x 32 x 8 banks),
178FBGA 11x11.5, 2/CS, 2CKE

2.0 KEY FEATURE

- Double-data rate architecture; two data transfers per clock cycle
- Bidirectional data strobes (DQS_t, DQS_c), These are transmitted/received with data to be used in capturing data at the receiver
- Differential clock inputs (CK_t and CK_c)
- Differential data strobes (DQS_t and DQS_c)
- Commands & addresses entered on both positive and negative CK edges; data and data mask referenced to both edges of DQS
- 8 internal banks for concurrent operation
- Data mask (DM) for write data
- Burst Length: 8
- Burst Type: Sequential
- Read & Write latency : Refer to Table 45 LPDDR3 AC Timing Table
- Auto Precharge option for each burst access
- Configurable Drive Strength
- All Bank Refresh, Per Bank Refresh and Self Refresh
- Partial Array Self Refresh and Temperature Compensated Self Refresh
- Write Leveling
- CA Calibration
- HSUL_12 compatible inputs
- VDD1/VDD2/VDDQ/VDDCA
: 1.8V/1.2V/1.2V / 1.2V
- No DLL : CK to DQS is not synchronized
- Edge aligned data output, center aligned data input
- Operating Temperature : -25 ~ 85°C
- 2/CS, 2CKE
- On Die Termination using ODT pin

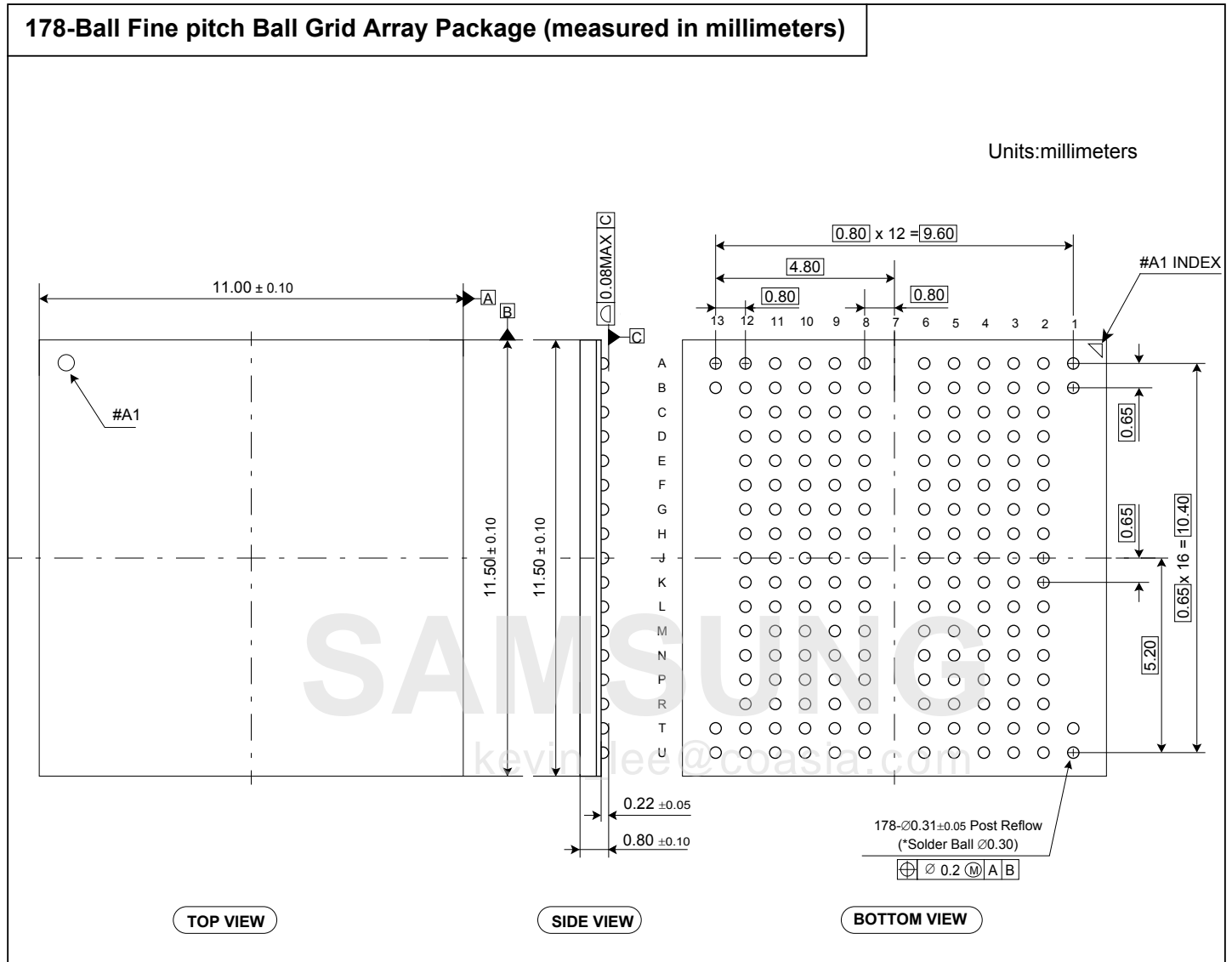
3.0 ORDERING INFORMATION

| Part No. | Org. | Package | Temperature | Max Frequency | Interface |
|-----------------|------|-----------------|-----------------|------------------------|-----------|
| K4E8E304EE-EGCF | x32 | 11x11.5 178FBGA | Tc = -25 ~ 85°C | 1866Mbps (tCK=1.075ns) | HSUL_12 |
| K4E8E304EE-EGCE | | | | 1600Mbps (tCK=1.25ns) | |

| K4 | E | 8E | 30 | 4 | E | E | - | E | G | CF/CE | |
|--|----------|-----------|-----------|----------|----------|----------|----------|----------|----------|--------------|---|
| Samsung Mobile DRAM Memory | | | | | | | | | | | Speed CF: 1.075ns@RL14, tRCD18ns, tRP18ns CE: 1.25ns@RL12, tRCD18ns, tRP18ns |
| Device Type E : LPDDR3 SDRAM | | | | | | | | | | | Temp, Power G : -25 ~ 85°C (Standard) |
| Density, Refresh 8E : 8G, 8K/32ms | | | | | | | | | | | Package E : 178-FBGA (HF, LF, 0.8x0.65pitch) |
| Organization 30 : x32 (2/CS, 2CKE) | | | | | | | | | | | Generation E : 6th Generation |
| Bank 4 : 8Bank | | | | | | | | | | | Interface, VDD, VDDQ E : HSUL_12, 1.8V, 1.2V, 1.2V, 1.2V |

4.0 PACKAGE DIMENSION & PIN DESCRIPTION

4.1 LPDDR3 SDRAM Package Dimension



4.2 LPDDR3 SDRAM Package Ballout

| 178Ball FBGA | | | | | | | | | | | | | |
|--------------|-----|-------|-------|----------|------|------|----|-------------------|------|--------|----------|------|-----|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 |
| A | DNU | DNU | VDD1 | VDD1 | VDD1 | VDD1 | NB | VDD2 | VDD2 | VDD1 | VDDQ | DNU | DNU |
| B | DNU | VSS | ZQ | NC | VSS | VSSQ | NB | DQ31 | DQ30 | DQ29 | DQ28 | VSSQ | DNU |
| C | | CA9 | VSSCA | NC | VSS | VSSQ | NB | DQ27 | DQ26 | DQ25 | DQ24 | VDDQ | |
| D | | CA8 | VSSCA | VDD2 | VDD2 | VDD2 | NB | DM3 | DQ15 | DQS3_t | DQS3_c | VSSQ | |
| E | | CA7 | CA6 | VSS | VSS | VSSQ | NB | VDDQ | DQ14 | DQ13 | DQ12 | VDDQ | |
| F | | VDDCA | CA5 | VSSCA | VSS | VSSQ | NB | DQ11 | DQ10 | DQ9 | DQ8 | VSSQ | |
| G | | VDDCA | VSSCA | VSSCA | VDD2 | VSSQ | NB | DM1 | VSSQ | DQS1_t | DQS1_c | VDDQ | |
| H | | VSS | VDDCA | VRef(CA) | VDD2 | VDD2 | NB | VDDQ | VDDQ | VSSQ | VDDQ | VDD2 | |
| J | | CK_c | CK_t | VSSCA | VDD2 | VDD2 | NB | ODT ¹⁾ | VDDQ | VDDQ | VRef(DQ) | VSS | |
| K | | VSS | CKE0 | CKE1 | VDD2 | VDD2 | NB | VDDQ | NC | VSSQ | VDDQ | VDD2 | |
| L | | VDDCA | CS0_n | CS1_n | VDD2 | VSS | NB | DM0 | VSSQ | DQS0_t | DQS0_c | VDDQ | |
| M | | VDDCA | CA4 | VSSCA | VSS | VSSQ | NB | DQ4 | DQ5 | DQ6 | DQ7 | VSSQ | |
| N | | CA2 | CA3 | VSS | VSS | VSSQ | NB | VDDQ | DQ1 | DQ2 | DQ3 | VDDQ | |
| P | | CA1 | VSSCA | VDD2 | VDD2 | VDD2 | NB | DM2 | DQ0 | DQS2_t | DQS2_c | VSSQ | |
| R | | CA0 | NC | VSS | VSS | VSSQ | NB | DQ20 | DQ21 | DQ22 | DQ23 | VDDQ | |
| T | DNU | VSS | VSS | VSS | VSS | VSSQ | NB | DQ16 | DQ17 | DQ18 | DQ19 | VSSQ | DNU |
| U | DNU | DNU | VDD1 | VDD1 | VDD1 | VDD1 | NB | VDD2 | VDD2 | VDD1 | VDDQ | DNU | DNU |

[Top View]

| | | | |
|--|-------|--|--------|
| | Power | | Ground |
| | ODT | | NB |
| | ZQ | | DNU/NC |

NOTE :

1) In case ODT function is not used, ODT pin should be considered as NC.

ODT will be connected to rank 0. The ODT Input to rank 1 (if 2nd rank is present) will be connected to Ground in the package.

4.3 LPDDR3 Pad Definition and Description

[Table 1] Pad Definition and Description

| Name | Type | Description |
|---|--------|---|
| CK_t, CK_c | Input | Clock: CK_t and CK_c are differential clock inputs. All Double Data Rate (DDR) CA inputs are sampled on both positive and negative edge of CK_t. Single Data Rate (SDR) inputs, CS_n and CKE, are sampled at the positive Clock edge. Clock is defined as the differential pair, CK_t and CK_c. The positive Clock edge is defined by the crosspoint of a rising CK_t and a falling CK_c. The negative Clock edge is defined by the cross point of a falling CK_t and a rising CK_c. |
| CKE0, CKE1 | Input | Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and therefore device input buffers and output drivers. Power savings modes are entered and exited through CKE transitions. CKE is considered part of the command code. See [Table 5] for command code descriptions. CKE is sampled at the positive Clock edge. |
| CS0_n, CS1_n | Input | Chip Select: CS_n is considered part of the command code. See [Table 5] for command code descriptions. CS_n is sampled at the positive Clock edge. |
| CA0 - CA9 | Input | DDR Command/Address Inputs: Uni-directional command/address bus inputs. CA is considered part of the command code. See [Table 5] for command code descriptions. |
| DQ0 - DQ31 (x32) | I/O | Data Inputs/Outputs: Bi-directional data bus |
| DQS0_t-DQS3_t DQS0_c-DQS3_c (x32) | I/O | Data Strobes (Bi-directional, Differential): The data strobe is bi-directional (used for read and write data) and differential (DQS_t and DQS_c). It is output with read data and input with write data. DQS is edge-aligned to read data and centered with write data. For x32, DQS0_t and DQS0_c correspond to the data on DQ0 - DQ7, DQS1_t and DQS1_c to the data on DQ8 - DQ15, DQS2_t and DQS2_c to the data on DQ16 - DQ23, DQS3_t and DQS3_c to the data on DQ24 - DQ31. |
| DM0 - DM3 (x32) | Input | Input Data Mask: DM is the input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM is for input only, the DM loading shall match the DQ and DQS_t (or DQS_c). For x32 device, DM0 is the input data mask signal for the data on DQ0-7, DM1 is the input data mask signal for the data on DQ8-15, DM2 is the input data mask signal for the data on DQ16-23 and DM3 is the input data mask signal for the data on DQ24-31. |
| ODT | Input | On Die Termination: This signal enables and disables termination on the DRAM DQ bus according to the specified mode register settings. |
| V _{DD1} | Supply | Core Power Supply 1: Core power supply. |
| V _{DD2} | Supply | Core Power Supply 2: Core power supply. |
| V _{DDCA} | Supply | Input Receiver Power Supply: Power supply for CA0-9, CKE, CS_n, CK_t, and CK_c input buffers. |
| V _{DDQ} | Supply | I/O Power Supply: Power supply for Data input/output buffers. |
| V _{REF} (CA) | Supply | Reference Voltage for CA Command and Control Input Receiver: Reference voltage for all CA0-9, CKE, CS_n, CK_t, and CK_c input buffers. |
| V _{REF} (DQ) | Supply | Reference Voltage for DQ Input Receiver: Reference voltage for all data input buffers. |
| V _{SS} | Supply | Ground |
| V _{SSCA} | Supply | Ground for Input Receivers |
| V _{SSQ} | Supply | I/O Ground: Ground for data input/output buffers |
| ZQ | I/O | Reference Pin for Output Drive Strength Calibration |

NOTE :

1) Data includes DQ and DM.

5.0 FUNCTIONAL DESCRIPTION

LPDDR3-SDRAM is a high-speed synchronous DRAM device internally configured as an 8-Bank memory.

This device contains the following number of bits:

4Gb has 4,294,967,296 bits

LPDDR3 devices use a double data rate architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus contains command, address, and bank information. Each command uses one clock cycle, during which command information is transferred on both the positive and negative edge of the clock.

These devices also use a double data rate architecture on the DQ pins to achieve high speed operation. The double data rate architecture is essentially an 8n prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR3 SDRAM effectively consists of a single 8n-bit wide, one clock cycle data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses to the LPDDR3 SDRAMs are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Activate command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the Activate command are used to select the row and the Bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the Bank and the starting column location for the burst access.

Prior to normal operation, the LPDDR3 SDRAM must be initialized. The following section provides detailed information covering device initialization, register definition, command description and device operation.

6.0 LPDDR3 SDRAM ADDRESSING

[Table 2] LPDDR3 SDRAM Addressing

| Items | | 4Gb |
|---------------------|--------------------------------|---------|
| Number of Banks | | 8 |
| Bank Addresses | | BA0-BA2 |
| $t_{REFI}(us)^{2)}$ | | 3.9 |
| x16 | Row Addresses | R0-R13 |
| | Column Addresses ¹⁾ | C0-C10 |
| x32 | Row Addresses | R0-R13 |
| | Column Addresses ¹⁾ | C0-C9 |

NOTE :

1) The least-significant column address C0 is not transmitted on the CA bus, and is implied to be zero.

2) t_{REFI} values for all bank refresh is $T_c = -25\sim 85^{\circ}C$, T_c means Operating Case Temperature

3) Row and Column Address values on the CA bus that are not used are "don't care."

6.1 Simplified LPDDR3 State Diagram

LPDDR3-SDRAM state diagram provides a simplified illustration of allowed state transitions and the related commands to control them. For a complete definition of the device behavior, the information provided by the state diagram should be integrated with the truth tables and timing specification.

The truth tables provide complementary information to the state diagram, they clarify the device behavior and the applied restrictions when considering the actual state of all the banks.

For the command definition, see datasheet of [Command Definition & Timing Diagram].

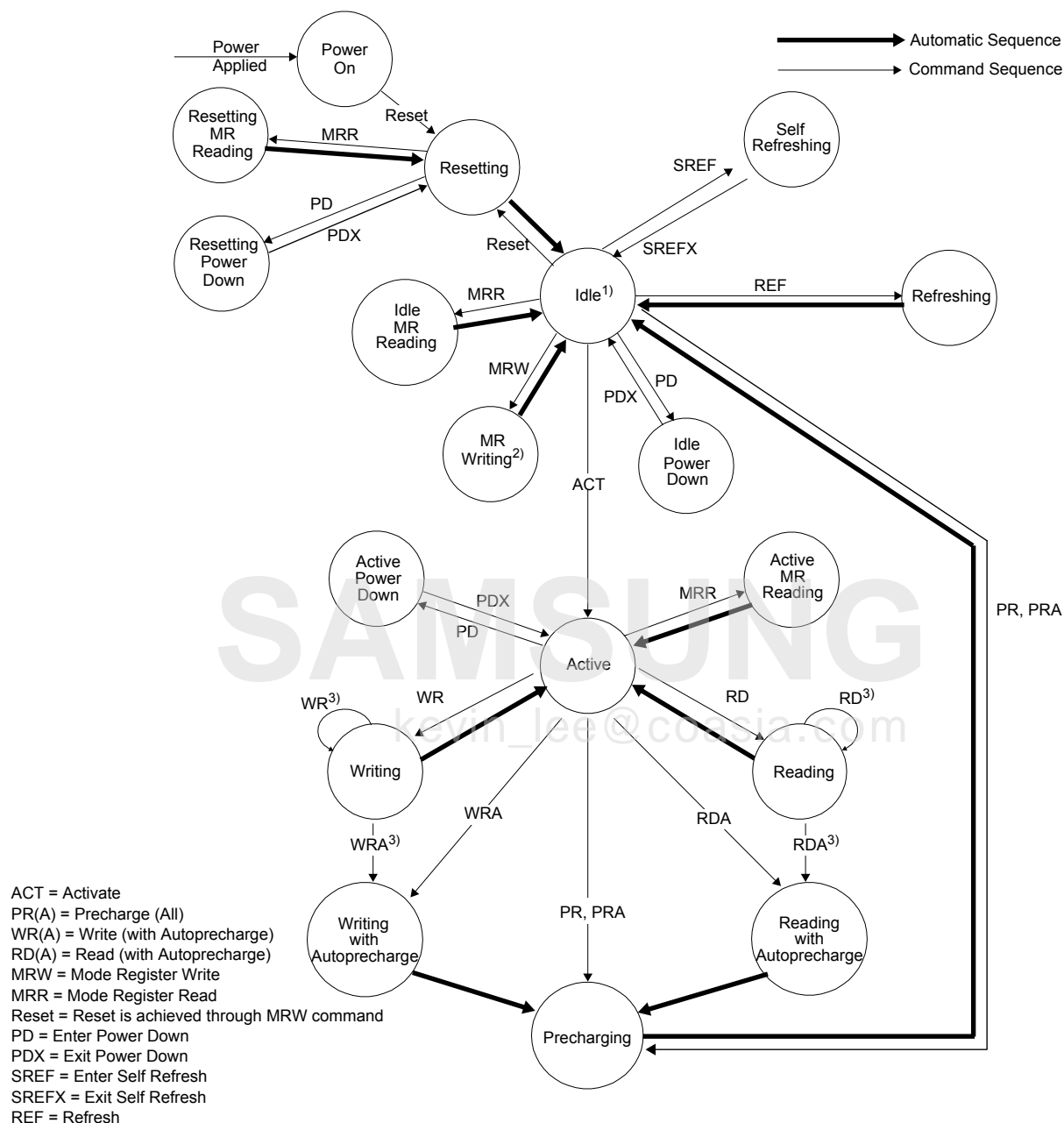


Figure 1. LPDDR3: Simplified Bus Interface State Diagram

NOTE :

1) In the Idle state, all banks are precharged.

2) In the case of MRW to enter CA Training mode or Write Leveling Mode, the state machine will not automatically return to the Idle state. In these cases an additional MRW command is required to exit either operating mode and return to the Idle state. See sections "CA Training" or "Write Leveling".

3) Terminated bursts are not allowed. For these state transitions, the burst operation must be completed before the transition can occur.

4) Use caution with this diagram. It is intended to provide a floorplan of the possible state transitions and commands to control them, not all details. In particular, situations involving more than one bank are not captured in full detail.

6.2 Mode Register Definition

6.2.1 Mode Register Assignment and Definition in LPDDR3 SDRAM

Table 3 shows the mode registers for LPDDR3 SDRAM. Each register is denoted as "R" if it can be read but not written, "W" if it can be written but not read, and "R/W" if it can be read and written. A Mode Register Read command is used to read a mode register. A Mode Register Write command is used to write a mode register.

[Table 3] Mode Register Assignment in LPDDR3 SDRAM

| MR# | MA <7:0> | Function | Access | OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|--------|----------------------------------|-----------------------------|--------|--|---------------|---------|--------------------|---------|--------------|--------|-----|
| 0 | 00 _H | Device Info. | R | (RFU) | WL (Set B) | (RFU) | RZQI (optional) | | (RFU) | | DAI |
| 1 | 01 _H | Device Feature 1 | W | nWR (for AP) | | | (RFU) | | BL | | |
| 2 | 02 _H | Device Feature 2 | W | WR Lev | WL Select | (RFU) | nWRE | RL & WL | | | |
| 3 | 03 _H | I/O Config-1 | W | (RFU) | | | | DS | | | |
| 4 | 04 _H | Refresh Rate | R | TUF | (RFU) | | | | Refresh Rate | | |
| 5 | 05 _H | Basic Config-1 | R | LPDDR3 Manufacturer ID | | | | | | | |
| 6 | 06 _H | Basic Config-2 | R | Revision ID1 | | | | | | | |
| 7 | 07 _H | Basic Config-3 | R | Revision ID2 | | | | | | | |
| 8 | 08 _H | Basic Config-4 | R | I/O width | | Density | | | | Type | |
| 9 | 09 _H | Test Mode | W | Vendor-Specific Test Mode | | | | | | | |
| 10 | 0A _H | IO Calibration | W | Calibration Code | | | | | | | |
| 11 | 0B _H | ODT Feature | | (RFU) | | | | | PD CTL | DQ ODT | |
| 12:15 | 0C _H ~0F _H | (Reserved) | | (RFU) | | | | | | | |
| 16 | 10 _H | PASR_Bank | W | PASR Bank Mask | | | | | | | |
| 17 | 11 _H | PASR_Seg | W | PASR Segment Mask | | | | | | | |
| 18-31 | 12 _H -1F _H | (Reserved) | | (RFU) | | | | | | | |
| 32 | 20 _H | DQ Calibration Pattern A | R | See "DQ Calibration" on Operations & Timing Diagram. | | | | | | | |
| 33:39 | 21 _H ~27 _H | (Do Not Use) | | | | | | | | | |
| 40 | 28 _H | DQ Calibration Pattern B | R | See "DQ Calibration" on Operations & Timing Diagram. | | | | | | | |
| 41 | 29 _H | CA Training 1 | W | See "Mode Register Write-CA Training Mode". | | | | | | | |
| 42 | 2A _H | CA Training 2 | W | See "Mode Register Write-CA Training Mode". | | | | | | | |
| 43:47 | 2B _H ~2F _H | (Do Not Use) | | | | | | | | | |
| 48 | 30 _H | CA Training 3 | W | See "Mode Register Write-CA Training Mode". | | | | | | | |
| 49:62 | 31 _H ~3E _H | (Reserved) | | (RFU) | | | | | | | |
| 63 | 3F _H | Reset | W | X | | | | | | | |
| 64:255 | 40 _H ~FF _H | (Reserved) | | (RFU) | | | | | | | |

NOTE :

- 1) RFU bits shall be set to '0' during Mode Register writes.
- 2) RFU bits shall be read as '0' during Mode Register reads.
- 3) All Mode Registers that are specified as RFU or write-only shall return undefined data when read and DQS_t, DQS_c shall be toggled.
- 4) All Mode Registers that are specified as RFU shall not be written.
- 5) See vendor device datasheets for details on vendor-specific mode registers.
- 6) Writes to read-only registers shall have no impact on the functionality of the device.

MR0_Device Information (MA<7:0> = 00_H) :

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|-------|--------------------|-------|--------------------|-----|-------|-----|-----|
| (RFU) | WL (Set B) Support | (RFU) | RZQI (Optional) | | (RFU) | | DAI |

| | | | | |
|---|-----------|---------|---|------------------------------------|
| DAI (Device Auto-Initialization Status) | Read-only | OP<0> | 0 _B : DAI complete 1 _B : DAI still in progress | |
| RZQI (Built in Self Test for RZQ Information) | Read-only | OP<4:3> | 00 _B : RZQ self test not supported 01 _B : ZQ-pin may connect to VDDCA or float 10 _B : ZQ-pin may short to GND 11 _B : ZQ-pin self test completed, no error condition detected (ZQ-pin may not connect to VDDCA or float nor short to GND) | 1-4 |
| WL (Set B) Support | Read-only | OP<6> | 0 _B : DRAM does not support WL (Set B) 1 _B : DRAM supports WL (SetB) | WL (Set B) Option Support |

NOTE :

- 1) RZQI, if supported, will be set upon completion of the MRW ZQ Initialization Calibration command.
- 2) If ZQ is connected to VDDCA to set default calibration, OP[4:3] shall be set to 01. If ZQ is not connected to VDDCA, either OP[4:3] = 01 or OP[4:3] = 10 might indicate a ZQ-pin assembly error. It is recommended that the assembly error is corrected.
- 3) In the case of possible assembly error (either OP[4:3]=01 or OP[4:3]=10 per Note 4), the LPDDR3 device will default to factory trim settings for RON, and will ignore ZQ calibration commands. In either case, the system may not function as intended.
- 4) In the case of the ZQ self-test returning a value of 11b, this result indicates that the device has detected a resistor connection to the ZQ pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e 240-Ω +/- 1%).

MR1_Device Feature 1 (MA<7:0> = 01_H) :

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|--------------|-----|-----|-------|-----|-----|-----|-----|
| nWR (for AP) | | | (RFU) | | BL | | |

| | | | |
|-------------------|------------|---------|---|
| BL | Write-only | OP<2:0> | 011 _B : BL8 (default) All others: Reserved |
| nWR ¹⁾ | Write-only | OP<7:5> | If nWRE (MR2 OP<4>) = 0: 100 _B : nWR=6 110 _B : nWR=8 111 _B : nWR=9 If nWRE (MR2 OP<4>) = 1: 000 _B : nWR=10 (default) 001 _B : nWR=11 010 _B : nWR=12 100 _B : nWR=14 110 _B : nWR=16 All others: Reserved |

NOTE :

- 1) Programmed value in nWR register is the number of clock cycles which determines when to start internal precharge operation for a write burst with AP enabled. It is determined by RU(tWR/tCK).

[Table 4] Burst Sequence

| C2 | C1 | C0 | BL | Burst Cycle Number and Burst Address Sequence | | | | | | | |
|----------------|----------------|----------------|----|---|---|---|---|---|---|---|---|
| | | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| 0 _B | 0 _B | 0 _B | 8 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 0 _B | 1 _B | 0 _B | | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 |
| 1 _B | 0 _B | 0 _B | | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 |
| 1 _B | 1 _B | 0 _B | | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 |

NOTE :

- 1) C0 input is not present on CA bus. It is implied zero.
- 2) The burst address represents C2 - C0.

MR2_Device Feature 2 (MA<7:0> = 02_H):

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|--------|-----------|-------|------|---------|-----|-----|-----|
| WR Lev | WL Select | (RFU) | nWRE | RL & WL | | | |

| | | | |
|-------------|------------|---------|---|
| RL & WL | Write-only | OP<3:0> | <p>If OP<6> = 0 (WL Set A, default) 0100_B: RL = 6 / WL = 3 (≤ 400 MHz) 0110_B: RL = 8 / WL = 4 (≤ 533 MHz) 0111_B: RL = 9 / WL = 5 (≤ 600 MHz) 1000_B: RL = 10 / WL = 6 (≤ 667 MHz, default) 1001_B: RL = 11 / WL = 6 (≤ 733 MHz) 1010_B: RL = 12 / WL = 6 (≤ 800 MHz) 1100_B: RL = 14 / WL = 8 (≤ 933 MHz) 1110_B: RL = 16 / WL = 8 (≤ 1066MHz) All others: Reserved</p> <p>If OP<6> = 1 (WL Set B, optional²⁾) 0100_B: RL = 6 / WL = 3 (≤ 400 MHz) 0110_B: RL = 8 / WL = 4 (≤ 533 MHz) 0111_B: RL = 9 / WL = 5 (≤ 600 MHz) 1000_B: RL = 10 / WL = 8 (≤ 667 MHz, default) 1001_B: RL = 11 / WL = 9 (≤ 733 MHz) 1010_B: RL = 12 / WL = 9 (≤ 800 MHz) 1100_B: RL = 14 / WL = 11 (≤ 933 MHz) 1110_B: RL = 16 / WL = 13 (≤ 1066MHz) All others: reserved</p> |
| nWRE | Write-only | OP<4> | <p>0_B : Enable nWR programming ≤ 9 1_B : Enable nWR programming > 9 (default)</p> |
| WL Select | Write-only | OP<6> | <p>0_B: Select WL Set A (default) 1_B: Select WL Set B (optional²⁾)</p> |
| WR Leveling | Write-only | OP<7> | <p>0_B : Disable (default) 1_B : Enable</p> |

NOTE :

1) See MR0, OP<7>

2) See MR0, OP<6>

MR3_I/O Configuration 1 (MA<7:0> = 03_H):

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|-------|-----|-----|-----|-----|-----|-----|-----|
| (RFU) | | | | DS | | | |

| | | | |
|----|------------|---------|--|
| DS | Write-only | OP<3:0> | <p>0001_B: 34.3-Ω typical pull-down/pull-up 0010_B: 40-Ω typical pull-down/pull-up (default) 0011_B: 48-Ω typical pull-down/pull-up 0100_B: Reserved for 60Ω typical pull-down/pull-up 0110_B: Reserved for 80Ω typical pull-down/pull-up 1001_B: 34.3Ω typical pull-down, 40Ω typical pull-up 1010_B: 40Ω typical pull-down, 48Ω typical pull-up 1011_B: 34.3Ω typical pull-down, 48Ω typical pull-up All others: Reserved</p> |
|----|------------|---------|--|

MR4_Device Temperature (MA<7:0> = 04_H)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|-----|-------|-----|-----|-----|--------------------|-----|-----|
| TUF | (RFU) | | | | SDRAM Refresh Rate | | |

| | | | |
|-------------------------------|-----------|---------|---|
| SDRAM Refresh Rate | Read-only | OP<2:0> | 000_B : SDRAM Low temperature operating limit exceeded 001_B : $4 \times t_{REFI}$, $4 \times t_{REFIpb}$, $4 \times t_{REFW}$ 010_B : $2 \times t_{REFI}$, $2 \times t_{REFIpb}$, $2 \times t_{REFW}$ 011_B : $1 \times t_{REFI}$, $1 \times t_{REFIpb}$, $1 \times t_{REFW}$ ($\leq 85^{\circ}\text{C}$) 100_B : $0.5 \times t_{REFI}$, $0.5 \times t_{REFIpb}$, $0.5 \times t_{REFW}$, do not de-rate SDRAM AC timing 101_B : $0.25 \times t_{REFI}$, $0.25 \times t_{REFIpb}$, $0.25 \times t_{REFW}$, do not de-rate SDRAM AC timing 110_B : $0.25 \times t_{REFI}$, $0.25 \times t_{REFIpb}$, $0.25 \times t_{REFW}$, de-rate SDRAM AC timing 111_B : SDRAM High temperature operating limit exceeded |
| Temperature Update Flag (TUF) | Read-only | OP<7> | 0_B : OP<2:0> value has not changed since last read of MR4. 1_B : OP<2:0> value has changed since last read of MR4. |

NOTE :

- 1) A Mode Register Read from MR4 will reset OP7 to '0'.
- 2) OP7 is reset to '0' at power-up. OP[2:0] bits are undefined after power-up.
- 3) If OP2 equals '1', the device temperature is greater than 85°C.
- 4) OP7 is set to '1' if OP2:OP0 has changed at any time since the last read of MR4.
- 5) LPDDR3 SDRAM might not operate properly when OP[2:0] = 000_B or 111_B.
- 6) For specified operating temperature range and maximum operating temperature refer to Table 13 Operating Temperature Range.
- 7) LPDDR3 devices shall be de-rated by adding 1.875 ns to the following core timing parameters: tRCD, tRC, tRAS, tRP, and tRRD. tDQSCK shall be de-rated according to the tDQSCK de-rating in Table 45 LPDDR3 AC Timing Table. Prevailing clock frequency spec and related setup and hold timings shall remain unchanged.
- 8) See "Temperature Sensor" on [Command Definition & Timing Diagram] for information on the recommended frequency of reading MR4.

MR5_Basic Configuration 1 (MA<7:0> = 05_H):

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|------------------------|-----|-----|-----|-----|-----|-----|-----|
| LPDDR3 Manufacturer ID | | | | | | | |

| | | | |
|------------------------|-----------|---------|--|
| LPDDR3 Manufacturer ID | Read-only | OP<7:0> | 0000 0000_B : Reserved 0000 0001_B : Samsung 0000 0010_B : Do Not Use 0000 0011_B : Do Not Use 0000 0100_B : Do Not Use 0000 0101_B : Do Not Use 0000 0110_B : Do Not Use 0000 0111_B : Do Not Use 0000 1000_B : Do Not Use 0000 1001_B : Do Not Use 0000 1010_B : Reserved 0000 1011_B : Do Not Use 0000 1100_B : Do Not Use 0000 1101_B : Do Not Use 0000 1110_B : Do Not Use 0000 1111_B : Do Not Use 1111 1110_B : Do Not Use All others : Reserved |
|------------------------|-----------|---------|--|

MR6_Basic Configuration 2 (MA<7:0> = 06_H):

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|--------------|-----|-----|-----|-----|-----|-----|-----|
| Revision ID1 | | | | | | | |

| | | | |
|--------------|-----------|---------|---|
| Revision ID1 | Read-only | OP<7:0> | 00000100_B : E-version |
|--------------|-----------|---------|---|

NOTE :

- 1) MR6 is vendor specific.

MR7_Basic Configuration 3 (MA<7:0> = 07_H):

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|--------------|-----|-----|-----|-----|-----|-----|-----|
| Revision ID2 | | | | | | | |

| | | | |
|--------------|-----------|---------|-----------------------------------|
| Revision ID2 | Read-only | OP<7:0> | 00000000 _B : A-version |
|--------------|-----------|---------|-----------------------------------|

NOTE :

1) MR7 is vendor specific.

MR8_Basic Configuration 4 (MA<7:0> = 08_H) :

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|-----------|-----|---------|-----|-----|-----|------|-----|
| I/O width | | Density | | | | Type | |

| | | | |
|-----------|-----------|---------|---|
| Type | Read-only | OP<1:0> | 11 _B : S8 SDRAM All others : Reserved |
| Density | Read-only | OP<5:2> | 0110 _B : 4Gb 1110 _B : 6Gb 0111 _B : 8Gb 1101 _B : 12Gb 1000 _B : 16Gb 1001 _B : 32Gb all others: Reserved |
| I/O width | Read-only | OP<7:6> | 00 _B : x32 01 _B : x16 All Others : Reserved |

MR9_Test Mode (MA<7:0> = 09_H):

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---------------------------|-----|-----|-----|-----|-----|-----|-----|
| Vendor-specific Test Mode | | | | | | | |

MR10_Calibration (MA<7:0> = 0A_H):

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|------------------|-----|-----|-----|-----|-----|-----|-----|
| Calibration Code | | | | | | | |

| | | | |
|------------------|------------|---------|---|
| Calibration Code | Write-only | OP<7:0> | 0xFF: Calibration command after initialization 0xAB: Long calibration 0x56: Short calibration 0xC3: ZQ Reset others: Reserved |
|------------------|------------|---------|---|

NOTE :

- Host processor shall not write MR10 with "Reserved" values.
- LPDDR3 devices shall ignore calibration command when a "Reserved" value is written into MR10.
- See AC timing table for the calibration latency.
- If ZQ is connected to V_{SSCA} through RZQ, either the ZQ calibration function (see Mode Register Write ZQ Calibration Command) or default calibration (through the ZQ_{RESET} command) is supported. If ZQ is connected to V_{DDCA}, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection shall not change after power is applied to the device.
- LPDDR3 devices that do not support calibration shall ignore the ZQ Calibration command.
- Optionally, the MRW ZQ Initialization Calibration command will update MR0 to indicate RZQ pin connection.

MR11_ODT Control (MA<7:0> = 0B_H):

| OP7 | | OP6 | | OP5 | | OP4 | | OP3 | | OP2 | | OP1 | | OP0 | |
|------------|------------|-----|---------|-----|---|-----|--|-----|--|--------|--|--------|--|-----|--|
| RFU | | | | | | | | | | PD CTL | | DQ ODT | | | |
| DQ ODT | Write-only | | OP<1:0> | | 00 _B : Disable (Default) 01 _B : RZQ/4 10 _B : RZQ/2 11 _B : RZQ/1 | | | | | | | | | | |
| PD Control | Write-only | | OP<2> | | 0 _B : ODT disabled by DRAM during power down (default) 1 _B : ODT enabled by DRAM during power down | | | | | | | | | | |

MR12:15_(Reserved) (MA<7:0> = 0C_H-0F_H):MR16_PASR_Bank Mask (MA<7:0> = 010_H):

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|-----------------|------------|---------|--|-----|-----|-----|-----|
| Bank Mask | | | | | | | |
| Bank <7:0> Mask | Write-only | OP<7:0> | 0_B : refresh enable to the bank (=unmasked, default) 1_B : refresh blocked (=masked) | | | | |

| OP | Bank Mask | 8-Bank SDRAM |
|----|-----------|--------------|
| 0 | XXXXXXX1 | Bank 0 |
| 1 | XXXXXX1X | Bank 1 |
| 2 | XXXXX1XX | Bank 2 |
| 3 | XXXX1XXX | Bank 3 |
| 4 | XXX1XXXX | Bank 4 |
| 5 | XX1XXXXX | Bank 5 |
| 6 | X1XXXXXX | Bank 6 |
| 7 | 1XXXXXXX | Bank 7 |

MR17_PASR_Segment Mask (MA<7:0> = 011_H):

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|-------------------|------------|---------|---|-----|-----|-----|-----|
| Segment Mask | | | | | | | |
| Segment <7:0>Mask | Write-only | OP<7:0> | 0_B : refresh enable to the segment (=unmasked, default) 1_B : refresh blocked (=masked) | | | | |

| Segment | OP | Segment Mask | 4Gb |
|---------|----|--------------|------------------------|
| | | | R13:11 |
| 0 | 0 | XXXXXXX1 | 000_B |
| 1 | 1 | XXXXXX1X | 001_B |
| 2 | 2 | XXXXX1XX | 010_B |
| 3 | 3 | XXXX1XXX | 011_B |
| 4 | 4 | XXX1XXXX | 100_B |
| 5 | 5 | XX1XXXXX | 101_B |
| 6 | 6 | X1XXXXXX | 110_B |
| 7 | 7 | 1XXXXXXX | 111_B |

NOTE :

1) This table indicates the range of row addresses in each masked segment. X is do not care for a particular segment.

MR18:31_(Reserved) (MA<7:0> = 012_H - 01F_H):

MR32_DQ Calibration Pattern A (MA<7:0>=20_H):

Reads to MR32 return DQ Calibration Pattern "A". See "DQ Calibration" on Operations & Timing Diagram.

MR33:39_(Do Not Use) (MA<7:0> = 21_H-27_H):

MR40_DQ Calibration Pattern B (MA<7:0>=28_H):

Reads to MR40 return DQ Calibration Pattern "B". See "DQ Calibration" on Operations & Timing Diagram.

MR41_CA Training 1 (MA<7:0> = 29_H):

Writes to MR41 enables CA Training. See Mode Register Write - CA Training Mode

MR42_CA Training 2 (MA<7:0> = 2A_H):

Writes to MR42 exits CA Training. See Mode Register Write - CA Training Mode

MR43:47_(Do Not Use)(MA<7:0> = 2B_H-2F_H):

MR48_CA Training_3 (MA<7:0>=30_H)

Writes to MR48 enables CA Training. See Mode Register Write - CA Training Mode

MR49:62_(Reserved) (MA<7:0> = 31_H - 3E_H) :

MR63_Reset (MA<7:0> = 3F_H): MRW only

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|-------------------------|-----|-----|-----|-----|-----|-----|-----|
| X or 0xFC ¹⁾ | | | | | | | |

NOTE :

1) For additional information on MRW RESET see "Mode Register Write Command" on [Command Definition & Timing Diagram].

MR64:255 (Reserved) (MA<7:0> = 40_H-FF_H) :

7.0 TRUTH TABLES

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR3 device must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

7.1 Command truth table

[Table 5] Command truth table

| | SDR Command Pins | | | DDR CA pins (10) | | | | | | | | | | | |
|---|------------------|-------|------|------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|---------|--|
| SDRAM Command | CKE | | CS_n | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 | CA6 | CA7 | CA8 | CA9 | CK EDGE | |
| | CK(n-1) | CK(n) | | | | | | | | | | | | | |
| MRW | H | H | L | L | L | L | L | MA0 | MA1 | MA2 | MA3 | MA4 | MA5 | | |
| | | | X | MA6 | MA7 | OP0 | OP1 | OP2 | OP3 | OP4 | OP5 | OP6 | OP7 | | |
| MRR | H | H | L | L | L | L | H | MA0 | MA1 | MA2 | MA3 | MA4 | MA5 | | |
| | | | X | MA6 | MA7 | X | | | | | | | | | |
| Refresh (per bank) | H | H | L | L | L | H | L | X | | | | | | | |
| | | | X | X | | | | | | | | | | | |
| Refresh (all bank) | H | H | L | L | L | H | H | X | | | | | | | |
| | | | X | X | | | | | | | | | | | |
| Enter Self Refresh | H | L | L | L | L | H | X | | | | | | | | |
| | X | | X | X | | | | | | | | | | | |
| Activate (bank) | H | H | L | L | H | R8 | R9 | R10 | R11 | R12 | BA0 | BA1 | BA2 | | |
| | | | X | R0 | R1 | R2 | R3 | R4 | R5 | R6 | R7 | R13 | R14 | | |
| Write (bank) | H | H | L | H | L | L | RFU | RFU | C1 | C2 | BA0 | BA1 | BA2 | | |
| | | | X | AP ³⁾ | C3 | C4 | C5 | C6 | C7 | C8 | C9 | C10 | C11 | | |
| Read (bank) | H | H | L | H | L | H | RFU | RFU | C1 | C2 | BA0 | BA1 | BA2 | | |
| | | | X | AP ³⁾ | C3 | C4 | C5 | C6 | C7 | C8 | C9 | C10 | C11 | | |
| Precharge ¹¹⁾ (pre bank, all bank) | H | H | L | H | H | L | H | AB | X | | | BA0 | BA1 | BA2 | |
| | | | X | X | | | | | | | | | | | |
| NOP | H | H | L | H | H | H | X | | | | | | | | |
| | | | X | X | | | | | | | | | | | |
| Maintain PD, SREF (NOP) ⁴⁾ | L | L | L | H | H | H | X | | | | | | | | |
| | | | X | X | | | | | | | | | | | |
| NOP | H | H | H | X | | | | | X | | | | | | |
| | | | X | X | | | | | | | | | | | |
| Maintain PD, SREF ⁴⁾ | L | L | X | X | | | | | | | | | | | |
| | | | X | X | | | | | | | | | | | |
| Enter Power Down | H | L | H | X | | | | | X | | | | | | |
| | X | | X | X | | | | | | | | | | | |
| Exit PD, SREF | L | H | H | X | | | | | X | | | | | | |
| | X | | X | X | | | | | | | | | | | |

NOTE:

- 1) All LPDDR3 commands are defined by states of CS_n, CA0, CA1, CA2, CA3, and CKE at the rising edge of the clock.
- 2) Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon.
- 3) AP "high" during a READ or WRITE command indicates that an auto-precharge will occur to the bank associated with the READ or WRITE command.
- 4) "X" means "H or L (but a defined logic level)", except when the LPDDR3 SDRAM is in PD, SREF in which case CS_n, CK_t/CK_c, and CA can be floated after the required tCPDED time is satisfied, and until the required exit procedure is initiated as described in the respective entry/exit procedure, See also Self-Refresh Operation and Basic Power-Down Entry and Exit Timing in LPDDR3 operations & Timing specification.
- 5) Self refresh exit is asynchronous.
- 6) V_{REF} must be between 0 and VDDQ during Self Refresh.
- 7) CAxr refers to command/address bit "x" on the rising edge of clock.
- 8) CAxf refers to command/address bit "x" on the falling edge of clock.
- 9) CS_n and CKE are sampled at the rising edge of clock.
- 10) The least-significant column address C0 is not transmitted on the CA bus, and is implied to be zero.
- 11) AB "high" during Precharge command indicates that all bank Precharge will occur. In this case, Bank Address is do-not-care.
- 12) When CS_n is HIGH, LPDDR3 CA bus can be floated.

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7.2 CKE Truth Table

[Table 6] LPDDR3 : CKE Table ^{1), 2)}

| Device Current State ³⁾ | CKE _{n-1} ⁴⁾ | CKE _n ⁴⁾ | CS _n ⁵⁾ | Command n ⁶⁾ | Operation ⁶⁾ | Device Next State | Notes |
|------------------------------------|----------------------------------|--------------------------------|----------------------------------|-------------------------|----------------------------------|-------------------------|-------|
| Active Power Down | L | L | X | X | Maintain Active Power Down | Active Power Down | |
| | L | H | H | NOP | Exit Active Power Down | Active | 7 |
| Idle Power Down | L | L | X | X | Maintain Idle Power Down | Idle Power Down | |
| | L | H | H | NOP | Exit Idle Power Down | Idle | 7 |
| Resetting Power Down | L | L | X | X | Maintain Resetting Power Down | Resetting Power Down | |
| | L | H | H | NOP | Exit Resetting Power Down | Idle or Resetting | 7, 9 |
| Self Refresh | L | L | X | X | Maintain Self Refresh | Self Refresh | |
| | L | H | H | NOP | Exit Self Refresh | Idle | 8 |
| Bank(s) Active | H | L | H | NOP | Enter Active Power Down | Active Power Down | |
| All Banks Idle | H | L | H | NOP | Enter Idle Power Down | Idle Power Down | |
| | H | L | L | Enter Self-Refresh | Enter Self Refresh | Self Refresh | |
| Resetting | H | L | H | NOP | Enter Resetting Power Down | Resetting Power Down | |
| | H | H | Refer to the Command Truth Table | | | | |

NOTE :

- 1) All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
- 2) 'X' means 'Don't care'.
- 3) "Current state" is the state of the LPDDR3 device immediately prior to clock edge n.
- 4) "CKE_n" is the logic state of CKE at clock rising edge n; "CKE_{n-1}" was the state of CKE at the previous clock edge.
- 5) "CS_n" is the logic state of CS_n at the clock rising edge n;
- 6) "Command n" is the command registered at clock edge N, and "Operation n" is a result of "Command n".
- 7) Power Down exit time (t_{XP}) should elapse before a command other than NOP is issued. The clock must toggle at least twice during the t_{XP} period.
- 8) Self-Refresh exit time (t_{XSR}) should elapse before a command other than NOP is issued. The clock must toggle at least twice during the t_{XSR} time.
- 9) Upon exiting Resetting Power Down, the device will return to the Idle state if tINIT5 has expired.
- 10) In the case of ODT disabled, all DQ output shall be Hi-Z. In the case of ODT enabled, all DQ shall be terminated to VDDQ.

7.3 State Truth Table

The truth tables provide complementary information to the state diagram, they clarify the device behavior and the applied restrictions when considering the actual state of all banks.

[Table 7] Current State Bank n - Command to Bank n

| Current State | Command | Operation | Next State | NOTES |
|---------------|--------------------|--|-----------------------|------------|
| Any | NOP | Continue previous operation | Current State | |
| Idle | ACTIVATE | Select and activate row | Active | |
| | Refresh (Per Bank) | Begin to refresh | Refreshing (Per Bank) | 6 |
| | Refresh (All Bank) | Begin to refresh | Refreshing (All Bank) | 7 |
| | MRW | Write value to Mode Register | MR Writing | 7 |
| | MRR | Read value from Mode Register | Idle MR Reading | |
| | Reset | Begin Device Auto-Initialization | Resetting | 8 |
| | Precharge | Deactivate row in bank or banks | Precharging | 9, 14 |
| Row Active | Read | Select column, and start read burst | Reading | 11 |
| | Write | Select column, and start write burst | Writing | 11 |
| | MRR | Read value from Mode Register | Active MR Reading | |
| | Precharge | Deactivate row in bank or banks | Precharging | 9 |
| Reading | Read | Select column, and start new read burst | Reading | 10, 11 |
| | Write | Select column, and start write burst | Writing | 10, 11, 12 |
| Writing | Write | Select column, and start new write burst | Writing | 10, 11 |
| | Read | Select column, and start read burst | Reading | 10, 11, 13 |
| Power On | Reset | Begin Device Auto-Initialization | Resetting | 8 |
| Resetting | MRR | Read value from Mode Register | Resetting MR Reading | |

NOTE :

- The table applies when both CKEn-1 and CKEn are HIGH, and after t_{XSR} or t_{XP} has been met if the previous state was Power Down.
- All states and sequences not shown are illegal or reserved.
- Current State Definitions:
 - Idle: The bank or banks have been precharged, and t_{RP} has been met.
 - Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts / accesses and no register accesses are in progress.
 - Reading: A Read burst has been initiated, with Auto Precharge disabled.
 - Writing: A Write burst has been initiated, with Auto Precharge disabled.
- The following states must not be interrupted by a command issued to the same bank. NOP commands or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other banks are determined by its current state and Table 1, and according to Table 2.
 - Precharging: starts with the registration of a Precharge command and ends when t_{RP} is met. Once t_{RP} is met, the bank will be in the idle state.
 - Row Activating: starts with registration of an Activate command and ends when t_{RCD} is met. Once t_{RCD} is met, the bank will be in the 'Active' state.
 - Read with AP Enabled: starts with the registration of the Read command with Auto Precharge enabled and ends when t_{RP} has been met. Once t_{RP} has been met, the bank will be in the idle state.
 - Write with AP Enabled: starts with registration of a Write command with Auto Precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank will be in the idle state.
- The following states must not be interrupted by any executable command; NOP commands must be applied to each positive clock edge during these states.
 - Refreshing (Per Bank): starts with registration of a Refresh (Per Bank) command and ends when t_{RFCpb} is met. Once t_{RFCpb} is met, the bank will be in an 'idle' state.
 - Refreshing (All Bank): starts with registration of an Refresh (All Bank) command and ends when t_{RFCab} is met. Once t_{RFCab} is met, the device will be in an 'all banks idle' state.
 - Idle MR Reading: starts with the registration of a MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the bank will be in the Idle state.
 - Resetting MR Reading: starts with the registration of a MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the bank will be in the Resetting state.
 - Active MR Reading: starts with the registration of a MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the bank will be in the Active state.
 - MR Writing: starts with the registration of a MRW command and ends when t_{MRW} has been met. Once t_{MRW} has been met, the bank will be in the Idle state.
 - Precharging All: starts with the registration of a Precharge-All command and ends when t_{RP} is met. Once t_{RP} is met, the bank will be in the idle state.
- Bank-specific; requires that the bank is idle and no bursts are in progress.
- Not bank-specific; requires that all banks are idle and no bursts are in progress.
- Not bank-specific reset command is achieved through Mode Register Write command.
- This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
- A command other than NOP should not be issued to the same bank while a Read or Write burst with Auto Precharge is enabled.
- The new Read or Write command could be Auto Precharge enabled or Auto Precharge disabled.
- A Write command may be applied after the completion of the Read burst; burst terminates are not permitted.
- A Read command may be applied after the completion of the Write burst; burst terminates are not permitted.
- If a Precharge command is issued to a bank in the Idle state, t_{RP} shall still apply.

[Table 8] Current State Bank n - Command to Bank m

| Current State of Bank n | Command for Bank m | Operation | Next State for Bank m | NOTES |
|--|--------------------|---|--------------------------------------|---------|
| Any | NOP | Continue previous operation | Current State of Bank m | |
| Idle | Any | Any command allowed to Bank m | - | |
| Row Activating, Active, or Precharging | Activate | Select and activate row in Bank m | Active | 6 |
| | Read | Select column, and start read burst from Bank m | Reading | 7 |
| | Write | Select column, and start write burst to Bank m | Writing | 7 |
| | Precharge | Deactivate row in bank or banks | Precharging | 8 |
| | MRR | Read value from Mode Register | Idle MR Reading or Active MR Reading | 9,10,12 |
| Reading (Autoprecharge disabled) | Read | Select column, and start read burst from Bank m | Reading | 7 |
| | Write | Select column, and start write burst to Bank m | Writing | 7,13 |
| | Activate | Select and activate row in Bank m | Active | |
| | Precharge | Deactivate row in bank or banks | Precharging | 8 |
| Writing (Autoprecharge disabled) | Read | Select column, and start read burst from Bank m | Reading | 7,15 |
| | Write | Select column, and start write burst to Bank m | Writing | 7 |
| | Activate | Select and activate row in Bank m | Active | |
| | Precharge | Deactivate row in bank or banks | Precharging | 8 |
| Reading with Autoprecharge | Read | Select column, and start read burst from Bank m | Reading | 7,14 |
| | Write | Select column, and start write burst to Bank m | Writing | 7,13,14 |
| | Activate | Select and activate row in Bank m | Active | |
| | Precharge | Deactivate row in bank or banks | Precharging | 8 |
| Writing with Autoprecharge | Read | Select column, and start read burst from Bank m | Reading | 7,14,15 |
| | Write | Select column, and start write burst to Bank m | Writing | 7,14 |
| | Activate | Select and activate row in Bank m | Active | |
| | Precharge | Deactivate row in bank or banks | Precharging | 8 |
| Power On | Reset | Begin Device Auto-Initialization | Resetting | 11,16 |
| Resetting | MRR | Read value from Mode Register | Resetting MR Reading | |

NOTE :

- The table applies when both CKEn-1 and CKEn are HIGH, and after t_{XSR} or t_{XP} has been met if the previous state was Self Refresh or Power Down.
- All states and sequences not shown are illegal or reserved.
- Current State Definitions:
 - Idle: The bank has been precharged, and TRP has been met.
 - Active: A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.
 - Reading: A Read burst has been initiated, with Auto Precharge disabled.
 - Writing: A Write burst has been initiated, with Auto Precharge disabled
- Refresh, Self-Refresh, and Mode Register Write commands may only be issued when all bank are idle.
- The following states must not be interrupted by any executable command; NOP commands must be applied during each clock cycle while in these states:
 - Idle MR Reading: starts with the registration of a MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the bank will be in the Idle state.
 - Resetting MR Reading: starts with the registration of a MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the bank will be in the Resetting state.
 - Active MR Reading: starts with the registration of a MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the bank will be in the Active state.
 - MR Writing: starts with the registration of a MRW command and ends when t_{MRW} has been met. Once t_{MRW} has been met, the bank will be in the Idle state.
- t_{RRD} must be met between Activate command to Bank n and a subsequent Activate command to Bank m. Additionally, in the case of multiple banks activated, t_{FAW} must be satisfied.
- Reads or Writes listed in the Command column include Reads and Writes with Auto Precharge enabled and Reads and Writes with Auto Precharge disabled.
- This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
- MRR is allowed during the Row Activating state (Row Activating starts with registration of an Activate command and ends when t_{RCD} is met.)
- MRR is allowed during the Precharging state. (Precharging starts with registration of a Precharge command and ends when t_{RP} is met.)
- Not bank-specific; requires that all banks are idle and no bursts are in progress.
- The next state for Bank m depends on the current state of Bank m (Idle, Row Activating, Precharging, or Active). The reader shall note that the state may be in transition when a MRR is issued. Therefore, if Bank m is in the Row Activating state and Precharging, the next state may be Active and Precharge dependent upon t_{RCD} and t_{RP} respectively.
- A Write command may be applied after the completion of the Read burst, burst terminates are not permitted.
- Read with auto precharge enabled or a Write with Auto Precharge enabled may be followed by any valid command to other banks provided that the timing restrictions described in the Precharge & Auto Precharge clarification table are followed.
- A Read command may be applied after the completion of the Write burst, burst terminates are not permitted.
- Reset command is achieved through Mode Register Write command.

7.4 Data mask truth table

[Table 9] provides the data mask truth table.

[Table 9] DM truth table

| Name (Functional) | DM | DQs | Note |
|-------------------|----|-------|------|
| Write enable | L | Valid | 1 |
| Write inhibit | H | X | 1 |

NOTE :

1) Used to mask write data, provided coincident with the corresponding data.

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8.0 ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

[Table 10] Absolute Maximum DC Ratings

| Parameter | Symbol | Min | Max | Units | Notes |
|--|------------------------------------|------|-----|-------|-------|
| VDD1 supply voltage relative to VSS | VDD1 | -0.4 | 2.3 | V | 1 |
| VDD2 supply voltage relative to VSS | VDD2 | -0.4 | 1.6 | V | 1 |
| VDDCA supply voltage relative to VSSCA | VDDCA | -0.4 | 1.6 | V | 1,2 |
| VDDQ supply voltage relative to VSSQ | VDDQ | -0.4 | 1.6 | V | 1,3 |
| Voltage on any ball relative to VSS | V _{IN} , V _{OUT} | -0.4 | 1.6 | V | |
| Storage Temperature | T _{STG} | -55 | 125 | °C | 4 |

NOTE :

- 1) See Power Ramp for relationships between power supplies.
- 2) $V_{REPCA} \leq 0.6 \times VDDCA$; however, V_{REPCA} may be $\geq VDDCA$ provided that $V_{REPCA} \leq 300\text{mV}$.
- 3) $V_{REFDQ} \leq 0.7 \times VDDQ$; however, V_{REFDQ} may be $\geq VDDQ$ provided that $V_{REFDQ} \leq 300\text{mV}$.
- 4) Storage Temperature is the case surface temperature on the center/top side of LPDDR3 device. For the measurement conditions, please refer to JESD51-2 standard.

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9.0 AC & DC OPERATING CONDITIONS

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR3 Device must be powered down and then restarted through the specialized initialization sequence before normal operation can continue.

9.1 Recommended DC Operating Conditions

[Table 11] Recommended DC Operating Conditions

| Symbol | DRAM | LPDDR3 | | | Unit |
|--------|--------------------|--------|------|------|------|
| | | Min | Typ | Max | |
| VDD1 | Core Power1 | 1.70 | 1.80 | 1.95 | V |
| VDD2 | Core Power2 | 1.14 | 1.20 | 1.3 | V |
| VDDCA | Input Buffer Power | 1.14 | 1.20 | 1.3 | V |
| VDDQ | I/O Buffer Power | 1.14 | 1.20 | 1.3 | V |

NOTE :

- 1) VDD1 uses significantly less current than VDD2.
- 2) The voltage range is for DC voltage only. DC is defined as the voltage supplied at the DRAM and is inclusive of all noise up to 1MHz at the DRAM package ball.

9.2 Input Leakage Current

[Table 12] Input Leakage Current

| Parameter/Condition | Symbol | Min | Max | Unit | Notes |
|----------------------------------|------------|-----|-----|------|-------|
| Input Leakage current | I_L | -4 | 4 | uA | 1,2 |
| V_{Ref} supply leakage current | I_{VREF} | -2 | 2 | uA | 3,4 |

NOTE :

- 1) For CA, CKE, CS_n, CK_t, CK_c. Any input $0V \leq V_{IN} \leq VDDCA$ (All other pins not under test = 0V)
- 2) Although DM is for input only, the DM leakage shall match the DQ and DQS_t/DQS_c output leakage specification.
- 3) The minimum limit requirement is for testing purposes. The leakage current on V_{RefCA} and V_{RefDQ} pins should be minimal.
- 4) $V_{REFDQ} = VDDQ/2$ or $V_{REFCA} = VDDCA/2$. (All other pins not under test = 0V)

9.3 Operating Temperature Range

[Table 13] Operating Temperature Range

| Parameter/Condition | Symbol | Min | Max | Unit |
|---------------------|------------|-----|-----|------|
| Standard | T_{OPER} | -25 | 85 | °C |

NOTE :

- 1) Operating Temperature is the case surface temperature on the center top side of the LPDDR3 device. For the measurement conditions, please refer to JESD51-2 standard.
- 2) Either the device case temperature rating or the temperature sensor (See "Temperature Sensor" on [Command Definition & Timing Diagram]) may be used to set an appropriate refresh rate, determine the need for AC timing de-rating and/or monitor the operating temperature. When using the temperature sensor, the actual device case temperature may be higher than the T_{OPER} rating that applies for the Standard or Extended Temperature Ranges. For example, T_{CASE} may be above 85°C when the temperature sensor indicates a temperature of less than 85°C.

10.0 AC AND DC INPUT MEASUREMENT LEVELS

10.1 AC and DC Logic Input Levels for Single-Ended Signals

10.1.1 AC and DC Input Levels for Single-Ended CA and CS_n Signals

[Table 14] Single-Ended AC and DC Input Levels for CA and CS_n inputs

| Symbol | Parameter | 1600 | | 1866 | | Unit | Notes |
|-------------------------|--|--------------------------|--------------------------|--------------------------|--------------------------|------|-------|
| | | Min | Max | Min | Max | | |
| V _{IHCA} (AC) | AC input logic high | V _{REF} + 0.150 | Note 2 | V _{REF} + 0.135 | Note 2 | V | 1, 2 |
| V _{ILCA} (AC) | AC input logic low | Note 2 | V _{REF} - 0.150 | Note 2 | V _{REF} - 0.135 | V | 1, 2 |
| V _{IHCA} (DC) | DC input logic high | V _{REF} + 0.100 | VDDCA | V _{REF} + 0.100 | VDDCA | V | 1 |
| V _{ILCA} (DC) | DC input logic low | VSSCA | V _{REF} - 0.100 | VSSCA | V _{REF} - 0.100 | V | 1 |
| V _{RefCA} (DC) | Reference Voltage for CA and CS_n inputs | 0.49 × VDDCA | 0.51 × VDDCA | 0.49 × VDDCA | 0.51 × VDDCA | V | 3, 4 |

NOTE :

- 1) For CA and CS_n input only pins. V_{Ref} = V_{RefCA}(DC).
- 2) See Overshoot and Undershoot Specifications.
- 3) The ac peak noise on V_{RefCA} may not allow V_{RefCA} to deviate from V_{RefCA}(DC) by more than +/-1% VDDCA (for reference: approx. +/- 12 mV).
- 4) For reference: approx. VDDCA/2 +/- 12 mV.

10.2 AC and DC Input Levels for CKE

[Table 15] Single-Ended AC and DC Input Levels for CKE

| Symbol | Parameter | Min | Max | Unit | Notes |
|--------------------|----------------------|--------------|--------------|------|-------|
| V _{IHCKE} | CKE Input High Level | 0.65 × VDDCA | Note 1 | V | 1 |
| V _{ILCKE} | CKE Input Low Level | Note 1 | 0.35 × VDDCA | V | 1 |

NOTE :

- 1) See Overshoot and Undershoot Specifications.

10.2.1 AC and DC Input Levels for Single-Ended Data Signals

[Table 16] Single-Ended AC and DC Input Levels for DQ and DM

| Symbol | Parameter | 1600 | | 1866 | | Unit | Notes |
|--|-------------------------------------|------------------------------------|------------------------------------|------------------------------------|------------------------------------|------|---------|
| | | Min | Max | Min | Max | | |
| V _{IHDQ} (AC) | AC input logic high | V _{REF} + 0.150 | Note 2 | V _{REF} + 0.135 | Note 2 | V | 1, 2, 5 |
| V _{ILDQ} (AC) | AC input logic low | Note 2 | V _{REF} - 0.150 | Note 2 | V _{REF} - 0.135 | V | 1, 2, 5 |
| V _{IHDQ} (DC) | DC input logic high | V _{REF} + 0.100 | VDDQ | V _{REF} + 0.100 | VDDQ | V | 1 |
| V _{ILDQ} (DC) | DC input logic low | VSSQ | V _{REF} - 0.100 | VSSQ | V _{REF} - 0.100 | V | 1 |
| V _{RefDQ} (DC) (DQ ODT disabled) | Reference Voltage for DQ, DM inputs | 0.49 × VDDQ | 0.51 × VDDQ | 0.49 × VDDQ | 0.51 × VDDQ | V | 3, 4 |
| V _{RefDQ} (DC) (DQ ODT enabled) | Reference Voltage for DQ, DM inputs | V _{ODTR} /2 - 0.01 × VDDQ | V _{ODTR} /2 + 0.01 × VDDQ | V _{ODTR} /2 - 0.01 × VDDQ | V _{ODTR} /2 + 0.01 × VDDQ | V | 3,5,6 |

NOTE :

- 1) For DQ input only pins. V_{ref} = V_{RefDQ}(DC).
- 2) See Overshoot and Undershoot Specifications.
- 3) The ac peak noise on V_{RefDQ} may not allow V_{RefDQ} to deviate from V_{RefDQ}(DC) by more than +/-1% VDDQ (for reference: approx. +/- 12 mV).
- 4) For reference : approx. VDDQ/2 +/- 12mV.
- 5) For reference : approx. V_{ODTR}/2 +/- 12mV.
- 6) The nominal mode register programmed value for RODT and the nominal controller output impedance RON are used for the calculation of V_{ODTR}. For testing purposes a controller RON value of 50Ω is used.

$$V_{ODTR} = \frac{2R_{ON} + R_{TT}}{R_{ON} + R_{TT}} \times V_{DDQ}$$

10.3 Vref Tolerances

The dc-tolerance limits and ac-noise limits for the reference voltages V_{RefCA} and V_{RefDQ} are illustrated in Figure 2. It shows a valid reference voltage $V_{\text{Ref}}(t)$ as a function of time. (V_{Ref} stands for V_{RefCA} and V_{RefDQ} likewise). VDD stands for VDDCA for V_{RefCA} and VDDQ for V_{RefDQ} . $V_{\text{Ref}}(\text{DC})$ is the linear average of $V_{\text{Ref}}(t)$ over a very long period of time (e.g. 1 sec) and is specified as a fraction of the linear average of VDDQ or VDDCA also over a very long period of time (e.g 1 sec). This average has to meet the min/max requirements in Table 14. Furthermore $V_{\text{Ref}}(t)$ may temporarily deviate from $V_{\text{Ref}}(\text{DC})$ by no more than $\pm 1\%$ VDD. $V_{\text{ref}}(t)$ cannot track noise on VDDQ or VDDCA if this would send Vref outside these specifications.

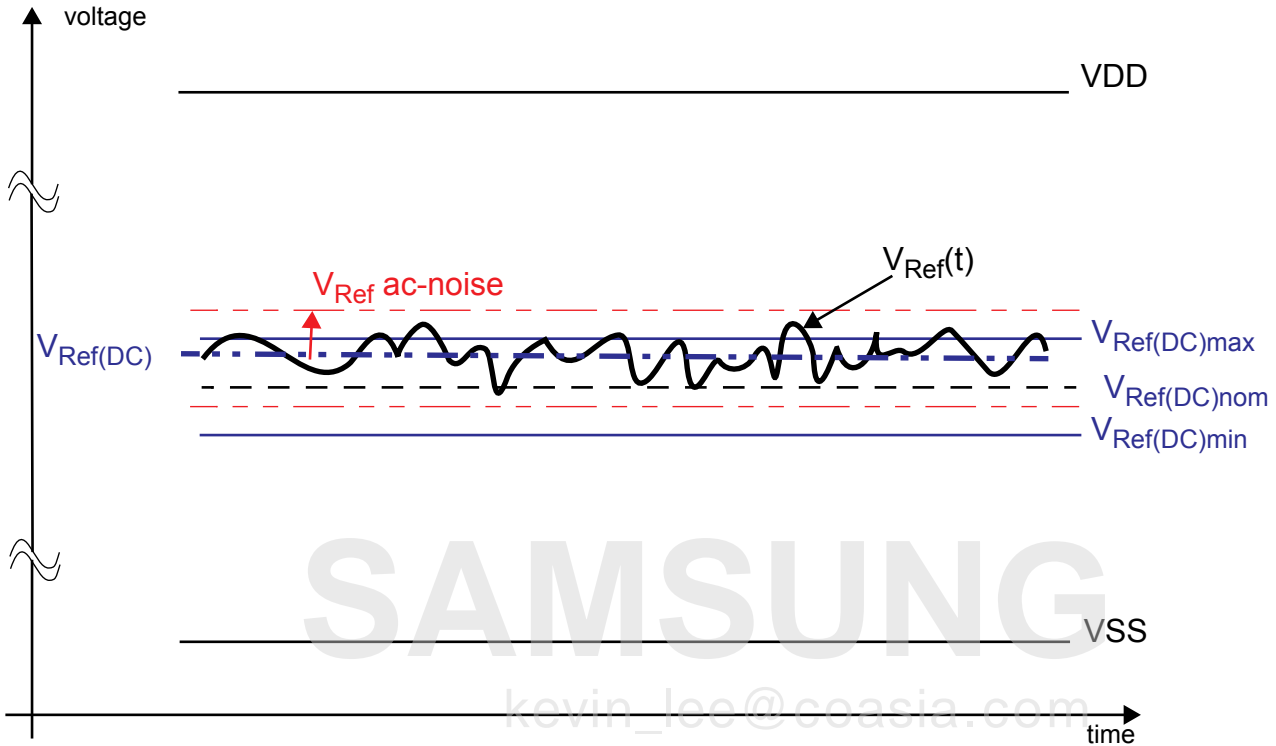


Figure 2. Illustration of $V_{\text{Ref}}(\text{DC})$ tolerance and V_{Ref} ac-noise limits

The voltage levels for setup and hold time measurements $V_{\text{IH}}(\text{AC})$, $V_{\text{IH}}(\text{DC})$, $V_{\text{IL}}(\text{AC})$ and $V_{\text{IL}}(\text{DC})$ are dependent on V_{Ref} .

" V_{Ref} " shall be understood as $V_{\text{Ref}}(\text{DC})$, as defined in Figure 2.

This clarifies that dc-variations of V_{Ref} affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for $V_{\text{Ref}}(\text{DC})$ deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the LPDDR3 setup/hold specification and derating values need to include time and voltage associated with V_{Ref} ac-noise. Timing and voltage effects due to ac-noise on V_{Ref} up to the specified limit ($\pm 1\%$ of VDD) are included in LPDDR3 timings and their associated deratings.

10.4 Input Signal

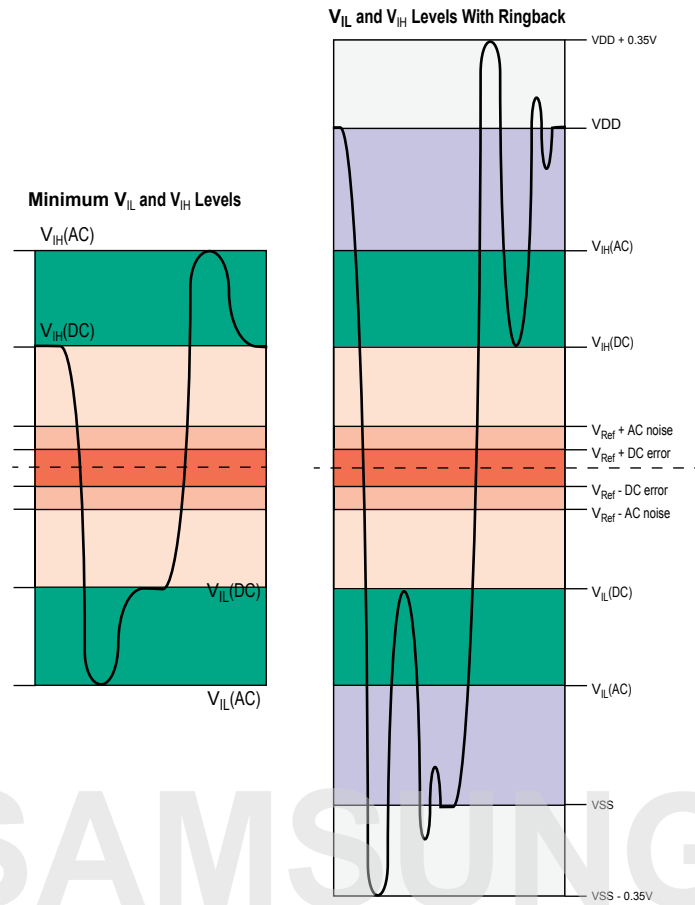


Figure 3. LPDDR3 Input Signal

NOTE :

- 1) Numbers reflect nominal values.
- 2) For CA0-9, CK_t, CK_c, and CS_n, VDD stands for VDDCA. For DQ, DM, DQS_t, and DQS_c, VDD stands for VDDQ.
- 3) For CA0-9, CK_t, CK_c, and CS_n, VSS stands for VSSCA. For DQ, DM, DQS_t, and DQS_c, VSS stands for VSSQ.

10.5.2 Differential swing requirements for clock (CK_t - CK_c) and strobe (DQS_t - DQS_c)

[Table 17] Differential AC and DC Input Levels

| Symbol | Parameter | Value | | Unit | Notes |
|------------------|----------------------------|-----------------------------------|-----------------------------------|------|-------|
| | | Min | Max | | |
| $V_{IHdiff}(DC)$ | Differential input high | $2 \times (V_{IH(dc)} - V_{ref})$ | Note 3 | V | 1 |
| $V_{ILdiff}(DC)$ | Differential input low | Note 3 | $2 \times (V_{IL(dc)} - V_{ref})$ | V | 1 |
| $V_{IHdiff}(AC)$ | Differential input high ac | $2 \times (V_{IH(ac)} - V_{ref})$ | Note 3 | V | 2 |
| $V_{ILdiff}(AC)$ | Differential input low ac | Note 3 | $2 \times (V_{IL(ac)} - V_{ref})$ | V | 2 |

NOTE :
 1)Used to define a differential signal slew-rate. For CK_t - CK_c use $V_{IH}/V_{IL}(dc)$ of CA and V_{REFCA} ; for DQS_t - DQS_c, use $V_{IH}/V_{IL}(DC)$ of DQs and V_{REFDQ} ; if a reduced dc-high or dc-low level is used for a signal group, then the reduced level applies also here.
 2)For CK_t - CK_c use $V_{IH}/V_{IL}(AC)$ of CA and V_{REFCA} ; for DQS_t - DQS_c, use $V_{IH}/V_{IL}(AC)$ of DQs and V_{REFDQ} ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
 3) These values are not defined, however the single-ended signals CK_t, CK_c, DQS_t, and DQS_c need to be within the respective limits ($V_{IH}(DC)$ max, $V_{IL}(DC)$ min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to Figure 10 Overshoot and Undershoot Definition.
 4) For CK_t and CK_c, $V_{ref} = V_{RefCA}(DC)$. For DQS_t and DQS_c, $V_{ref} = V_{RefDQ}(DC)$.

[Table 18] Allowed time before ringback tDVAC for DQS_t/DQS_c

| Slew Rate [V/ns] | tDVAC [ps] @ $ V_{IH/Ldiff}(AC) = 300mV$ 1600Mbps | | tDVAC [ps] @ $ V_{IH/Ldiff}(AC) = 270mV$ 1866Mbps | |
|------------------|--|-----|--|-----|
| | min | max | min | max |
| > 8.0 | 48 | - | 40 | - |
| 8.0 | 48 | - | 40 | - |
| 7.0 | 46 | - | 39 | - |
| 6.0 | 43 | - | 36 | - |
| 5.0 | 40 | - | 33 | - |
| 4.0 | 35 | - | 29 | - |
| 3.0 | 27 | - | 21 | - |
| < 3.0 | 27 | - | 21 | - |

[Table 19] Allowed time before ringback tDVAC for CK_t/CK_c

| Slew Rate [V/ns] | tDVAC [ps] @ $ V_{IH/Ldiff}(AC) = 300mV$ 1600Mbps | | tDVAC [ps] @ $ V_{IH/Ldiff}(AC) = 270mV$ 1866Mbps | |
|------------------|--|-----|--|-----|
| | min | max | min | max |
| > 8.0 | 48 | - | 40 | - |
| 8.0 | 48 | - | 40 | - |
| 7.0 | 46 | - | 39 | - |
| 6.0 | 43 | - | 36 | - |
| 5.0 | 40 | - | 33 | - |
| 4.0 | 35 | - | 29 | - |
| 3.0 | 27 | - | 21 | - |
| < 3.0 | 27 | - | 21 | - |

10.5.3 Single-ended requirements for differential signals

Each individual component of a differential signal (CK_t, DQS_t, CK_c, or DQS_c) has also to comply with certain requirements for single-ended signals. CK_t and CK_c shall meet $V_{SEH}(AC)_{min} / V_{SEL}(AC)_{max}$ in every half-cycle.

DQS_t, DQS_c shall meet $V_{SEH}(AC)_{min} / V_{SEL}(AC)_{max}$ in every half-cycle preceeding and following a valid transition.

Note that the applicable ac-levels for CA and DQ's are different per speed-bin.

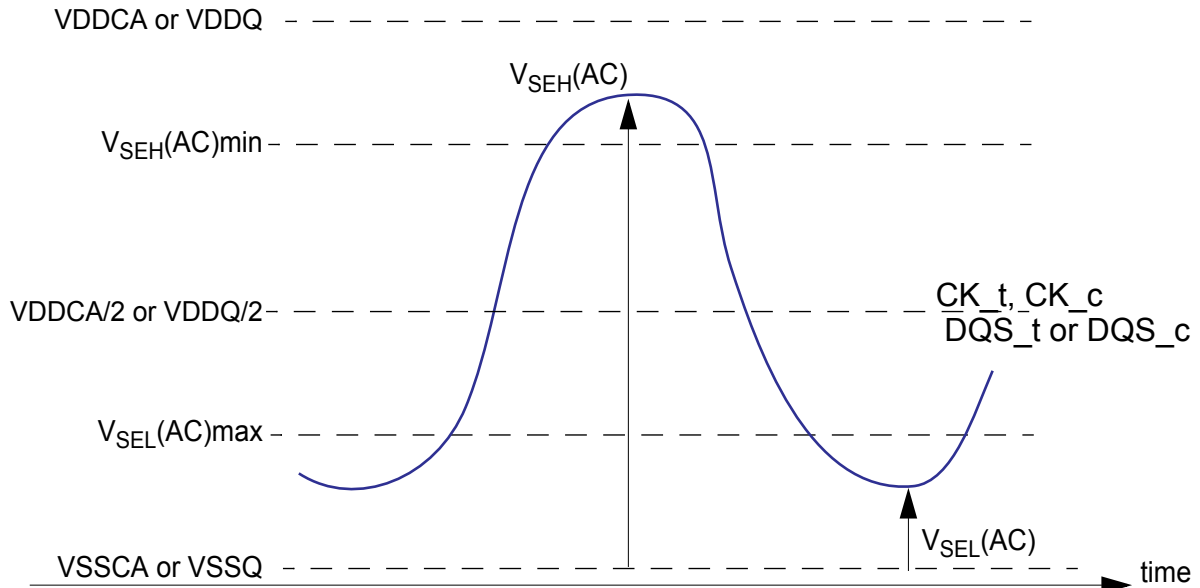


Figure 5. Single-ended requirement for differential signals.

Note that while CA and DQ signal requirements are with respect to Vref, the single-ended components of differential signals have a requirement with respect to VDDQ/2 for DQS_t, DQS_c and VDDCA/2 for CK_t, CK_c; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach $V_{SEL}(AC)_{max}$, $V_{SEH}(AC)_{min}$ has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

The single ended requirements for CK_t, CK_c, DQS_t and DQS_c are found in Table 14 and Table 16, respectively.

[Table 20] Single-ended levels for CK_t, DQS_t, CK_c, DQS_c

| Symbol | Parameter | Value | | Unit | Notes |
|----------------------|--|---------------------|---------------------|------|-------|
| | | Min | Max | | |
| V_{SEH} (AC150) | Single-ended high-level for strobes | (VDDQ/2)+0.150 | Note 3 | V | 1, 2 |
| | Single-ended high-level for CK_t, CK_c | (VDDCA/2)+0.150 | Note 3 | V | 1, 2 |
| V_{SEL} (AC150) | Single-ended low-level for strobes | Note 3 | (VDDQ/2)-0.150 | V | 1, 2 |
| | Single-ended low-level for CK_t, CK_c | Note 3 | (VDDCA/2)-0.150 | V | 1, 2 |
| V_{SEH} (AC135) | Single-ended high-level for strobes | (VDDQ / 2) + 0.135 | Note 3 | V | 1,2 |
| | Single-ended high-level for CK_t, CK_c | (VDDCA / 2) + 0.135 | Note 3 | V | 1,2 |
| V_{SEL} (AC135) | Single-ended low-level for strobes | Note 3 | (VDDQ / 2) - 0.135 | V | 1,2 |
| | Single-ended low-level for CK_t, CK_c | Note 3 | (VDDCA / 2) - 0.135 | V | 1,2 |

NOTE :

1) For CK_t, CK_c use $V_{SEH}/V_{SEL}(AC)$ of CA; for strobes (DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c) use $V_{IH}/V_{IL}(AC)$ of DQs.

2) $V_{IH}(AC)/V_{IL}(AC)$ for DQs is based on V_{RefDQ} ; $V_{SEH}(AC)/V_{SEL}(AC)$ for CA is based on V_{RefCA} ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.

3) These values are not defined, however the single-ended signals CK_t, CK_c, DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c need to be within the respective limits ($V_{IH}(DC)_{max}$, $V_{IL}(DC)_{min}$) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to Table 29, AC Overshoot/Undershoot Specification

10.6 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK_t, CK_c and DQS_t, DQS_c) must meet the requirements in Table 20. The differential input cross point voltage V_{IX} is measured from the actual cross point of true and complement signals to the mid-level between of VDD and VSS.

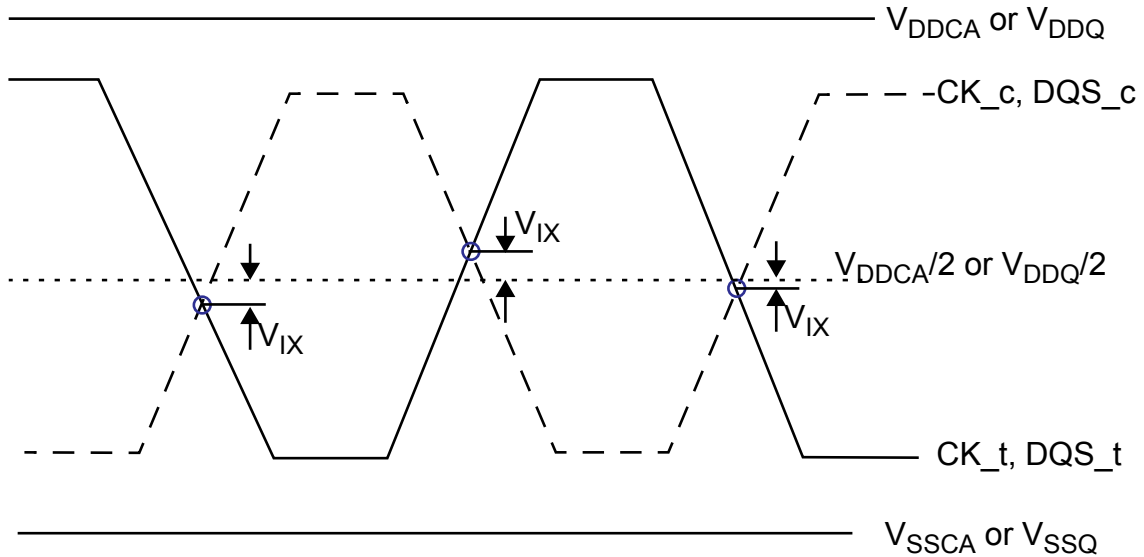


Figure 6. Vix Definition

[Table 21] Cross point voltage for differential input signals (CK, DQS)

| Symbol | Parameter | Value | | Unit | Notes |
|------------|---|-------|-----|------|-------|
| | | Min | Max | | |
| V_{IXCA} | Differential Input Cross Point Voltage relative to $V_{DDCA}/2$ for CK_t, CK_c | -120 | 120 | mV | 1,2 |
| V_{IXDQ} | Differential Input Cross Point Voltage relative to $V_{DDQ}/2$ for DQS_t, DQS_c | -120 | 120 | mV | 1,2 |

NOTE :

1) The typical value of $V_{IX(AC)}$ is expected to be about $0.5 \times V_{DD}$ of the transmitting device, and $V_{IX(AC)}$ is expected to track variations in VDD. $V_{IX(AC)}$ indicates the voltage at which differential input signals must cross.

2) For CK_t and CK_c, $V_{ref} = V_{RefCA(DC)}$. For DQS_t and DQS_c, $V_{ref} = V_{RefDQ(DC)}$.

10.7 Slew Rate Definitions for Single-Ended Input Signals

See CA and CS_n Setup, Hold and Derating for single-ended slew rate definitions for address and command signals.
See Data Setup, Hold and Slew Rate Derating for single-ended slew rate definitions for data signals.

10.8 Slew Rate Definitions for Differential Input Signals

Input slew rate for differential signals (CK_t, CK_c and DQS_t, DQS_c) are defined and measured as shown in Table 22 and Figure 7.

[Table 22] Differential Input Slew Rate Definition

| Description | Measured | | Defined by |
|---|------------------------|------------------------|--|
| | from | to | |
| Differential input slew rate for rising edge (CK_t - CK_c and DQS_t - DQS_c). | V _{ILdiffmax} | V _{IHdiffmin} | $[V_{IHdiffmin} - V_{ILdiffmax}] / \Delta TR_{diff}$ |
| Differential input slew rate for falling edge (CK_t - CK_c and DQS_t - DQS_c). | V _{IHdiffmin} | V _{ILdiffmax} | $[V_{IHdiffmin} - V_{ILdiffmax}] / \Delta TF_{diff}$ |

NOTE :
1) The differential signal (i.e. CK_t - CK_c and DQS_t - DQS_c) must be linear between these thresholds.

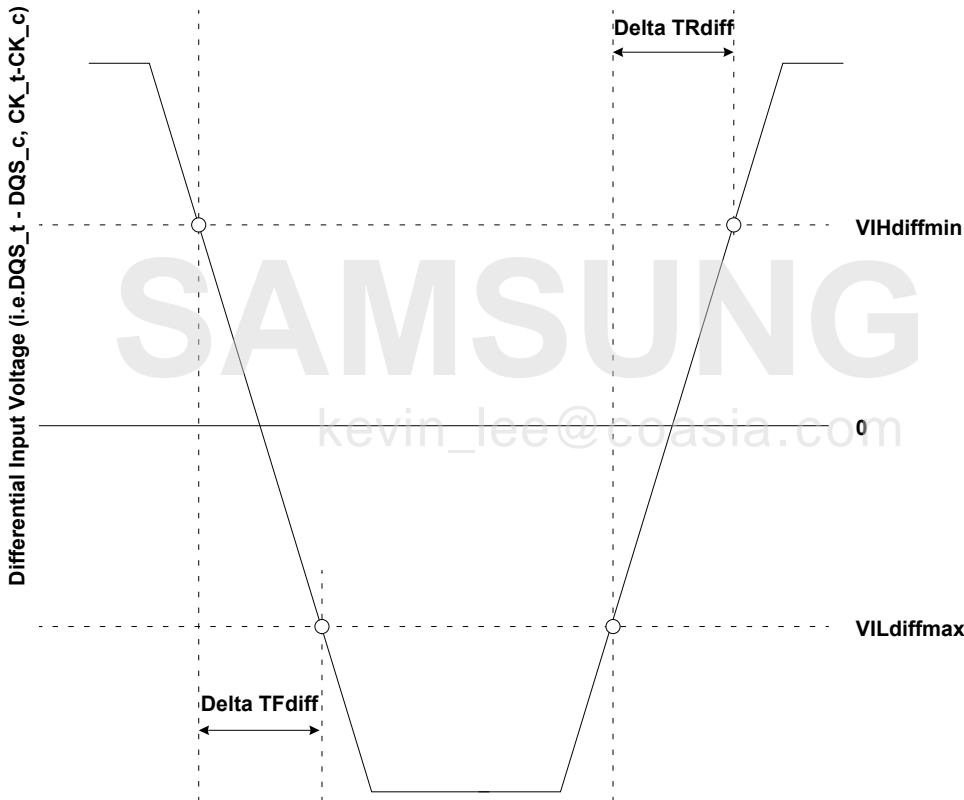


Figure 7. Differential Input Slew Rate Definition for DQS_t, DQS_c and CK_t, CK_c

11.0 AC AND DC OUTPUT MEASUREMENT LEVELS

11.1 Single Ended AC and DC Output Levels

Table 23 shows the output levels used for measurements of single ended signals.

[Table 23] Single-ended AC and DC Output Levels

| Symbol | Parameter | Value | Unit | Notes |
|------------------------------|---|--|------|-------|
| $V_{OH(DC)}$ | DC output high measurement level (for IV curve linearity) | $0.9 \times V_{DDQ}$ | V | 1 |
| $V_{OL(DC)}$ ODT disabled | DC output low measurement level (for IV curve linearity) | $0.1 \times V_{DDQ}$ | V | 2 |
| $V_{OL(DC)}$ ODT enabled | DC output low measurement level (for IV curve linearity) | $V_{DDQ} \times [0.1 + 0.9 \times (R_{ON} / R_{TT} + R_{ON})]$ | V | 3 |
| $V_{OH(AC)}$ | AC output high measurement level (for output slew rate) | $V_{RefDQ} + 0.12$ | V | |
| $V_{OL(AC)}$ | AC output low measurement level (for output slew rate) | $V_{RefDQ} - 0.12$ | V | |
| I_{OZ} | Output Leakage current (DQ, DM, DQS_t, DQS_c) (DQ, DQS_t, DQS_c are disabled; $0V \leq V_{OUT} \leq V_{DDQ}$) | Min | -10 | uA |
| | | Max | 10 | uA |
| MM _{PUPD} | Delta RON between pull-up and pull-down for DQ/DM | Min | -15 | % |
| | | Max | 15 | % |

NOTE :

1) $I_{OH} = -0.1mA$.

2) $I_{OL} = 0.1mA$.

3) The min value is derived when using RTT, min and RON,max (+/- 30% uncalibrated, +/- 15% calibrated).

11.2 Differential AC and DC Output Levels

Table 24 shows the output levels used for measurements of differential signals (DQS_t, DQS_c).

[Table 24] Differential AC and DC Output Levels

| Symbol | Parameter | Value | Unit | Notes |
|------------------|---|-------------------------|------|-------|
| $V_{OHdiff(AC)}$ | AC differential output high measurement level (for output SR) | $+ 0.20 \times V_{DDQ}$ | V | 1 |
| $V_{OLdiff(AC)}$ | AC differential output low measurement level (for output SR) | $- 0.20 \times V_{DDQ}$ | V | 2 |

NOTE :

1) $I_{OH} = -0.1mA$.

2) $I_{OL} = 0.1mA$.

11.3 Single Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single ended signals as shown in Table 25 and Figure 8.

[Table 25] Single-ended Output Slew Rate Definition

| Description | Measured | | Defined by |
|--|--------------|--------------|--|
| | from | to | |
| Single-ended output slew rate for rising edge | $V_{OL(AC)}$ | $V_{OH(AC)}$ | $[V_{OH(AC)} - V_{OL(AC)}] / \Delta t_{Rse}$ |
| Single-ended output slew rate for falling edge | $V_{OH(AC)}$ | $V_{OL(AC)}$ | $[V_{OH(AC)} - V_{OL(AC)}] / \Delta t_{Fse}$ |

NOTE :

1) Output slew rate is verified by design and characterization, and may not be subject to production test.

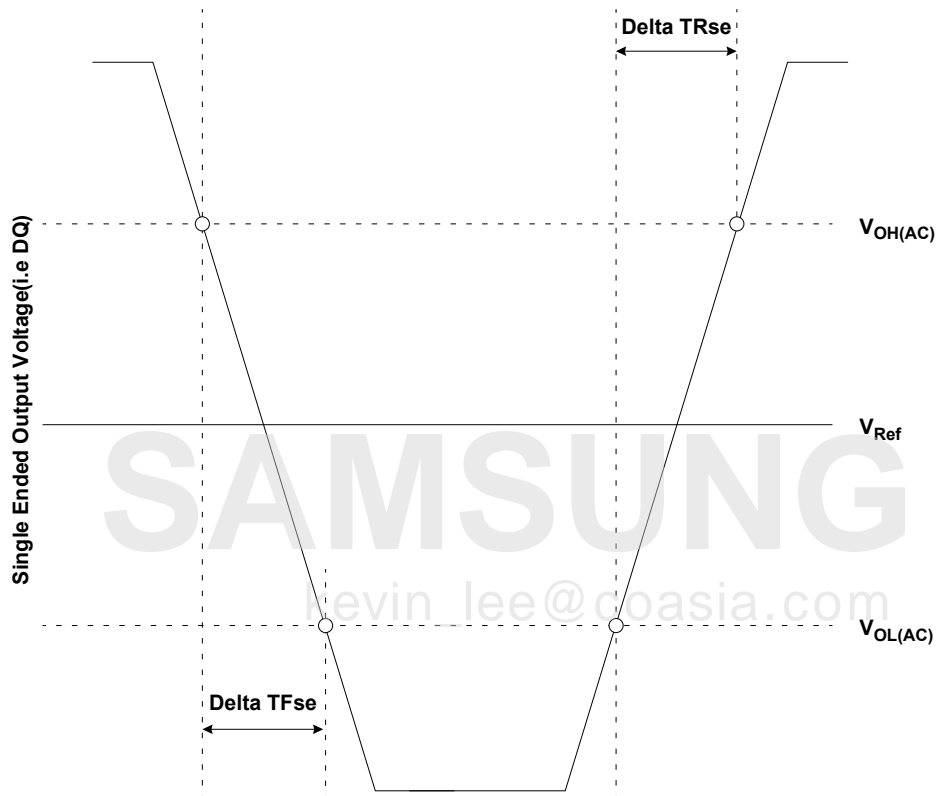


Figure 8. Single Ended Output Slew Rate Definition

[Table 26] Output Slew Rate (single-ended)

| Parameter | Symbol | Value | | Units |
|--|--------|-------------------|-------------------|-------|
| | | Min ¹⁾ | Max ²⁾ | |
| Single-ended Output Slew Rate ($R_{ON} = 40\Omega \pm 30\%$) | SRQse | 1.5 | 4.0 | V/ns |
| Output slew-rate matching Ratio (Pull-up to Pull-down) | | 0.7 | 1.4 | |

Description:

SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

se: Single-ended Signals

NOTE :

1) Measured with output reference load.

2) The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.

3) The output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$.

4) Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

11.4 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OLdiff}(AC)$ and $V_{OHdiff}(AC)$ for differential signals as shown in Table 27 and Figure 9.

[Table 27] Differential Output Slew Rate Definition

| Description | Measured | | Defined by |
|--|------------------|------------------|--|
| | from | to | |
| Differential output slew rate for rising edge | $V_{OLdiff}(AC)$ | $V_{OHdiff}(AC)$ | $[V_{OHdiff}(AC) - V_{OLdiff}(AC)] / \Delta TR_{diff}$ |
| Differential output slew rate for falling edge | $V_{OHdiff}(AC)$ | $V_{OLdiff}(AC)$ | $[V_{OHdiff}(AC) - V_{OLdiff}(AC)] / \Delta TF_{diff}$ |

NOTE :

1) Output slew rate is verified by design and characterization, and may not be subject to production test.

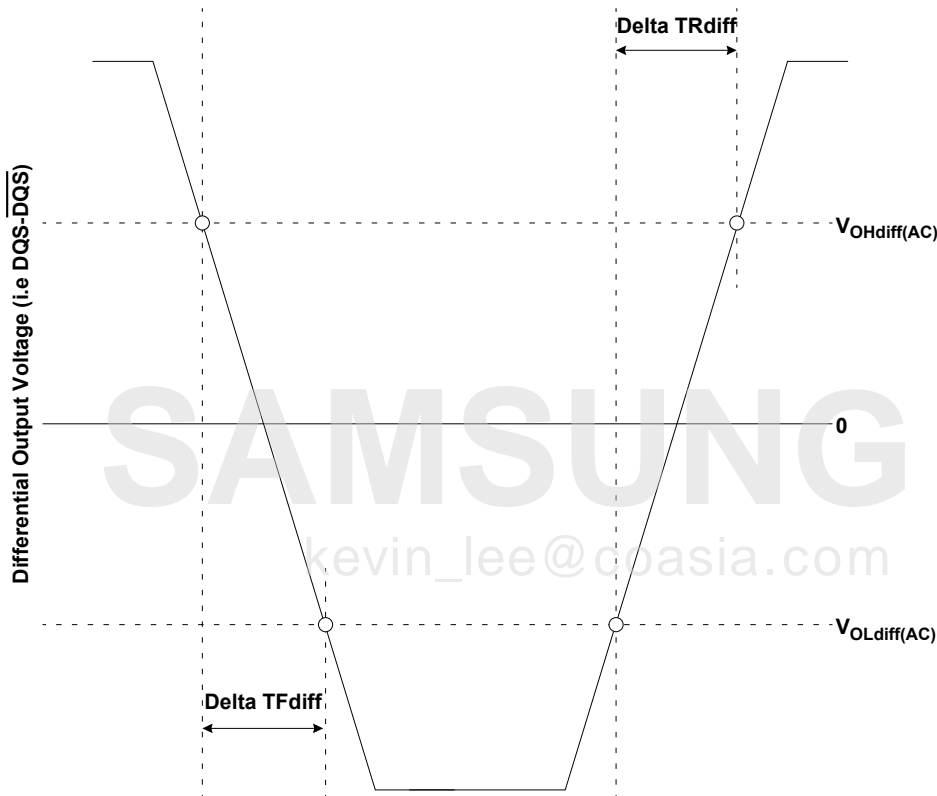


Figure 9. Differential Output Slew Rate Definition

[Table 28] Differential Output Slew Rate

| Parameter | Symbol | Value | | Units |
|--|---------|-------|-----|-------|
| | | Min | Max | |
| Differential Output Slew Rate ($R_{ON} = 40\Omega \pm 30\%$) | SRQdiff | 3.0 | 8.0 | V/ns |

Description:

SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

diff: Differential Signals

NOTE :

1) Measured with output reference load.

2) The output slew rate for falling and rising edges is defined and measured between $V_{OL}(AC)$ and $V_{OH}(AC)$.

3) Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

11.5 Overshoot and Undershoot Specifications

[Table 29] AC Overshoot/Undershoot Specification

| Parameter | | LPDDR3-1600 | LPDDR3-1866 | Units |
|--|-----|-------------|-------------|-------|
| Maximum peak amplitude allowed for overshoot area. (See Figure 10) | Max | 0.35 | | V |
| Maximum peak amplitude allowed for undershoot area. (See Figure 10) | Max | 0.35 | | V |
| Maximum area above VDD. (See Figure 10) | Max | 0.10 | | V-ns |
| Maximum area below VSS. (See Figure 10) | Max | 0.10 | | V-ns |

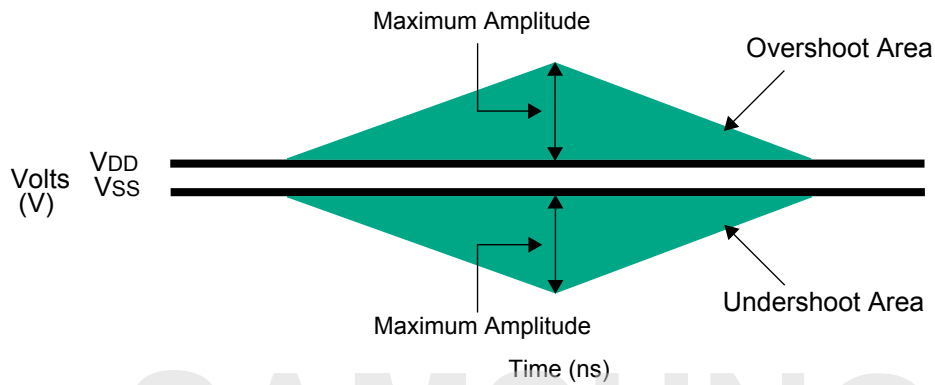


Figure 10. Overshoot and Undershoot Definition

NOTE :

- 1) VDD stands for VDDCA for CA[9:0], CK_t, CK_c, CS_n, and CKE. VDD stands for VDDQ for DQ, DM, ODT, DQS_t, and DQS_c.
- 2) VSS stands for VSSCA for CA[9:0], CK_t, CK_c, CS_n, and CKE. VSS stands for VSSQ for DQ, DM, ODT, DQS_t, and DQS_c.
- 3) Absolute maximum requirements apply.
- 4) Maximum peak amplitude values are referenced from actual VDD and VSS values.
- 5) Maximum area values are referenced from maximum operating VDD and VSS values.

12.0 OUTPUT BUFFER CHARACTERISTICS

12.1 HSUL_12 Driver Output Timing Reference Load

These 'Timing Reference Loads' are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

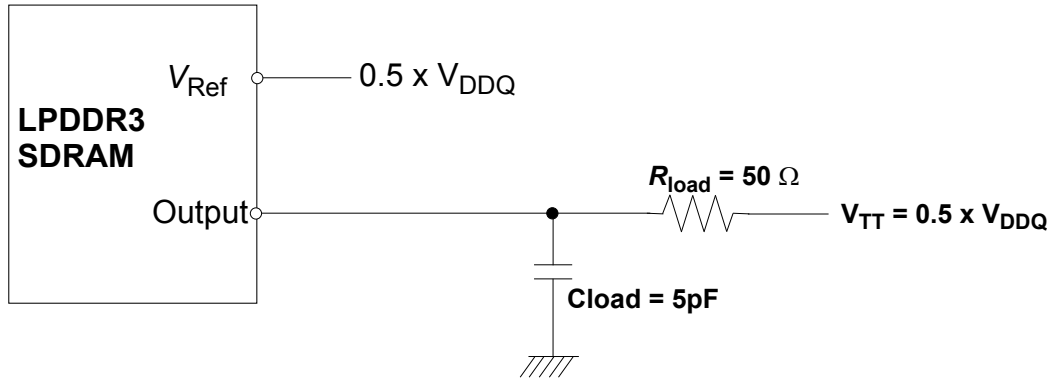


Figure 11. HSUL_12 Driver Output Reference Load for Timing and Slew Rate

NOTE :

1) All output timing parameter values (like t_{DQSQ} , t_{DQSQ} , t_{QHS} , t_{HZ} , t_{RPRE} etc.) are reported with respect to this reference load. This reference load is also used to report slew rate.

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13.0 R_{ONPU} AND R_{ONPD} RESISTOR DEFINITION

$$R_{ONPU} = \frac{(V_{DDQ} - V_{out})}{ABS(I_{out})}$$

NOTE :

1) This is under the condition that R_{ONPD} is turned off.

$$R_{ONPD} = \frac{V_{out}}{ABS(I_{out})}$$

NOTE :

1) This is under the condition that R_{ONPU} is turned off.

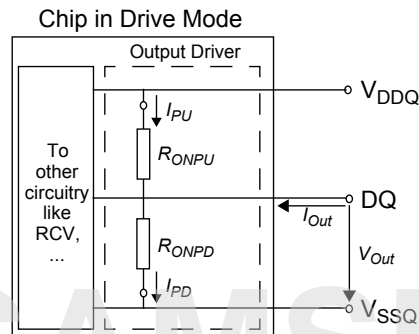


Figure 12. Output Driver: Definition of Voltages and Currents

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13.1 R_{ONPU} and R_{ONPD} Characteristics with ZQ Calibration

Output driver impedance R_{ON} is defined by the value of the external reference resistor R_{ZQ} . Nominal R_{ZQ} is 240Ω.

[Table 30] Output Driver DC Electrical Characteristics with ZQ Calibration

| R_{ONNOM} | Resistor | Vout | Min | Nom | Max | Unit | Notes |
|--|--------------|----------------------|--------|------|--------|------------|-------------|
| 34.3Ω | R_{ON34PD} | $0.5 \times V_{DDQ}$ | 0.85 | 1.00 | 1.15 | $R_{ZQ}/7$ | 1,2,3,4,6 |
| | R_{ON34PU} | $0.5 \times V_{DDQ}$ | 0.85 | 1.00 | 1.15 | $R_{ZQ}/7$ | 1,2,3,4,6 |
| 40.0Ω | R_{ON40PD} | $0.5 \times V_{DDQ}$ | 0.85 | 1.00 | 1.15 | $R_{ZQ}/6$ | 1,2,3,4,6 |
| | R_{ON40PU} | $0.5 \times V_{DDQ}$ | 0.85 | 1.00 | 1.15 | $R_{ZQ}/6$ | 1,2,3,4,6 |
| 48.0Ω | R_{ON48PD} | $0.5 \times V_{DDQ}$ | 0.85 | 1.00 | 1.15 | $R_{ZQ}/5$ | 1,2,3,4,6 |
| | R_{ON48PU} | $0.5 \times V_{DDQ}$ | 0.85 | 1.00 | 1.15 | $R_{ZQ}/5$ | 1,2,3,4,6 |
| Mismatch between pull-up and pull-down | MM_{PUPD} | | -15.00 | | +15.00 | % | 1,2,3,4,5,6 |

NOTE :

- 1) Across entire operating temperature range, after calibration.
- 2) $R_{ZQ} = 240\Omega$.
- 3) The tolerance limits are specified after calibration with fixed voltage and temperature. For behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
- 4) Pull-down and pull-up output driver impedances are recommended to be calibrated at $0.5 \times V_{DDQ}$.
- 5) Measurement definition for mismatch between pull-up and pull-down, MM_{PUPD} : Measure R_{ONPU} and R_{ONPD} , both at $0.5 \times V_{DDQ}$:

$$MM_{PUPD} = \frac{R_{ONPU} - R_{ONPD}}{R_{ONNOM}} \times 100$$

- For example, with $MM_{PUPD}(\max) = 15\%$ and $R_{ONPD} = 0.85$, R_{ONPU} must be less than 1.0
 6) Output driver strength measured without ODT.

13.2 Output Driver Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the Tables shown below.

[Table 31] Output Driver Sensitivity Definition

| Resistor | Vout | Min | Max | Unit | Notes |
|------------|-----------------|--|---|------|-------|
| R_{ONPD} | 0.5 x V_{DDQ} | $85 - (dRONdT \times \Delta T) - (dRONdV \times \Delta V)$ | $115 + (dRONdT \times \Delta T) + (dRONdV \times \Delta V)$ | % | 1,2 |
| R_{ONPU} | | | | | |
| R_{TT} | | $85 - (dRTTdT \times \Delta T) - (dRTTdV \times \Delta V)$ | $115 + (dRTTdT \times \Delta T) + (dRTTdV \times \Delta V)$ | | |

NOTE :

- 1) $\Delta T = T - T$ (@ calibration), $\Delta V = V - V$ (@ calibration)
- 2) $dRONdT$, $dRONdV$, $dRTTdV$, and $dRTTdT$ are not subject to production test but are verified by design and characterization.

[Table 32] Output Driver Temperature and Voltage Sensitivity

| Symbol | Parameter | Min | Max | Unit |
|----------|----------------------------------|------|------|--------|
| $dRONdT$ | R_{ON} Temperature Sensitivity | 0.00 | 0.75 | % / C |
| $dRONdV$ | R_{ON} Voltage Sensitivity | 0.00 | 0.20 | % / mV |
| $dRTTdT$ | R_{TT} Temperature Sensitivity | 0.00 | 0.75 | % / C |
| $dRTTdV$ | R_{TT} Voltage Sensitivity | 0.00 | 0.20 | % / mV |

13.3 R_{ONPU} and R_{ONPD} Characteristics without ZQ Calibration

Output driver impedance R_{ON} is defined by design and characterization as default setting.

[Table 33] Output Driver DC Electrical Characteristics without ZQ Calibration

| R_{ONNOM} | Resistor | Vout | Min | Nom | Max | Unit | Notes |
|---------------|--------------|-------------------|------|------|------|----------|-------|
| 34.3 Ω | R_{ON34PD} | $0.5 \times VDDQ$ | 24 | 34.3 | 44.6 | Ω | 1 |
| | R_{ON34PU} | $0.5 \times VDDQ$ | 24 | 34.3 | 44.6 | Ω | 1 |
| 40.0 Ω | R_{ON40PD} | $0.5 \times VDDQ$ | 28 | 40 | 52 | Ω | 1 |
| | R_{ON40PU} | $0.5 \times VDDQ$ | 28 | 40 | 52 | Ω | 1 |
| 48.0 Ω | R_{ON48PD} | $0.5 \times VDDQ$ | 33.6 | 48 | 62.4 | Ω | 1 |
| | R_{ON48PU} | $0.5 \times VDDQ$ | 33.6 | 48 | 62.4 | Ω | 1 |
| 60.0 Ω | R_{ON60PD} | $0.5 \times VDDQ$ | 42 | 60 | 78 | Ω | 1 |
| | R_{ON60PU} | $0.5 \times VDDQ$ | 42 | 60 | 78 | Ω | 1 |
| 80.0 Ω | R_{ON80PD} | $0.5 \times VDDQ$ | 56 | 80 | 104 | Ω | 1 |
| | R_{ON80PU} | $0.5 \times VDDQ$ | 56 | 80 | 104 | Ω | 1 |

NOTE:

1) Across entire operating temperature range, without calibration.

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13.4 RZQ I-V Curve

[Table 34] RZQ I-V Curve

| Voltage[V] | RON = 240Ω (RZQ) | | | | | | | |
|------------|-----------------------------|------|------------------|------|-----------------------------|-------|------------------|-------|
| | Pull-Down | | | | Pull-Up | | | |
| | Current [mA] / RON [Ohms] | | | | Current [mA] / RON [Ohms] | | | |
| | default value after ZQReset | | with Calibration | | default value after ZQReset | | with Calibration | |
| | Min | Max | Min | Max | Min | Max | Min | Max |
| | [mA] | [mA] | [mA] | [mA] | [mA] | [mA] | [mA] | [mA] |
| | | | | | | | | |
| 0.00 | 0.00 | 0.00 | n/a | n/a | 0.00 | 0.00 | n/a | n/a |
| 0.05 | 0.17 | 0.35 | n/a | n/a | -0.17 | -0.35 | n/a | n/a |
| 0.10 | 0.34 | 0.70 | n/a | n/a | -0.34 | -0.70 | n/a | n/a |
| 0.15 | 0.50 | 1.03 | n/a | n/a | -0.50 | -1.03 | n/a | n/a |
| 0.20 | 0.67 | 1.39 | n/a | n/a | -0.67 | -1.39 | n/a | n/a |
| 0.25 | 0.83 | 1.73 | n/a | n/a | -0.83 | -1.73 | n/a | n/a |
| 0.30 | 0.97 | 2.05 | n/a | n/a | -0.97 | -2.05 | n/a | n/a |
| 0.35 | 1.13 | 2.39 | n/a | n/a | -1.13 | -2.39 | n/a | n/a |
| 0.40 | 1.26 | 2.71 | n/a | n/a | -1.26 | -2.71 | n/a | n/a |
| 0.45 | 1.39 | 3.01 | n/a | n/a | -1.39 | -3.01 | n/a | n/a |
| 0.50 | 1.51 | 3.32 | n/a | n/a | -1.51 | -3.32 | n/a | n/a |
| 0.55 | 1.63 | 3.63 | n/a | n/a | -1.63 | -3.63 | n/a | n/a |
| 0.60 | 1.73 | 3.93 | 2.17 | 2.94 | -1.73 | -3.93 | -2.17 | -2.94 |
| 0.65 | 1.82 | 4.21 | n/a | n/a | -1.82 | -4.21 | n/a | n/a |
| 0.70 | 1.90 | 4.49 | n/a | n/a | -1.90 | -4.49 | n/a | n/a |
| 0.75 | 1.97 | 4.74 | n/a | n/a | -1.97 | -4.74 | n/a | n/a |
| 0.80 | 2.03 | 4.99 | n/a | n/a | -2.03 | -4.99 | n/a | n/a |
| 0.85 | 2.07 | 5.21 | n/a | n/a | -2.07 | -5.21 | n/a | n/a |
| 0.90 | 2.11 | 5.41 | n/a | n/a | -2.11 | -5.41 | n/a | n/a |
| 0.95 | 2.13 | 5.59 | n/a | n/a | -2.13 | -5.59 | n/a | n/a |
| 1.00 | 2.17 | 5.72 | n/a | n/a | -2.17 | -5.72 | n/a | n/a |
| 1.05 | 2.19 | 5.84 | n/a | n/a | -2.19 | -5.84 | n/a | n/a |
| 1.10 | 2.21 | 5.95 | n/a | n/a | -2.21 | -5.95 | n/a | n/a |
| 1.15 | 2.23 | 6.03 | n/a | n/a | -2.23 | -6.03 | n/a | n/a |
| 1.20 | 2.25 | 6.11 | n/a | n/a | -2.25 | -6.11 | n/a | n/a |

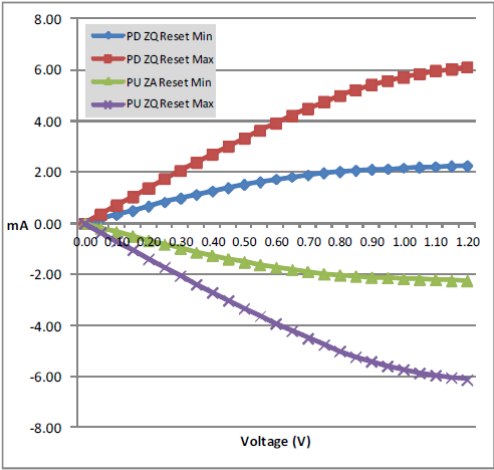


Figure 13. I-V Curve after ZQ Reset

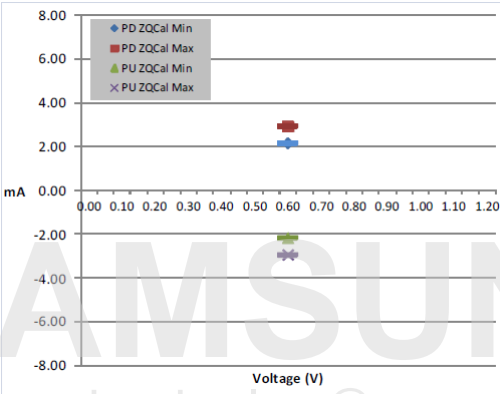
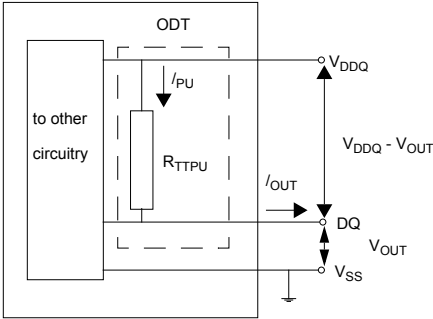


Figure 14. I-V Curve after Calibration

13.5 ODT Levels and I-V Characteristics

On-Die Termination effective resistance, R_{TT} , is defined by mode register MR11[1:0]. ODT is applied to the DQ, DM, and DQS_t/DQS_c pins. A functional representation of the on-die termination is shown in the figure below. R_{TT} is defined by the following formula:
 $R_{TTPU} = (V_{DDQ} - V_{OUT}) / |I_{OUT}|$



[Table 35] ODT DC Electrical Characteristics, assuming RZQ = 240 ohm after proper ZQ calibration

| R _{TT} (ohm) | V _{OUT} (V) | I _{OUT} | |
|-----------------------|----------------------|------------------|----------|
| | | Min (mA) | Max (mA) |
| RZQ/1 | 0.6 | -2.17 | -2.94 |
| RZQ/2 | 0.6 | -4.34 | -5.88 |
| RZQ/4 | 0.6 | -8.68 | -11.76 |

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14.0 INPUT/OUTPUT CAPACITANCE

[Table 36] Input/output capacitance

| Parameter | Symbol | | Value | Units | Notes |
|--|--------|-----|-------|-------|----------|
| Input capacitance, CK _t and CK _c | CCK | Min | 1.0 | pF | 1,2 |
| | | Max | 3.4 | pF | 1,2 |
| Input capacitance delta, CK _t and CK _c | CDCK | Min | 0.0 | pF | 1,2,3 |
| | | Max | 0.3 | pF | 1,2,3 |
| C _{in} , all other input-only pins except CS _n and CKE | CI1 | Min | 1.0 | pF | 1,2,4 |
| | | Max | 3.2 | pF | 1,2,4 |
| C _{in} , CS _{0_n} / CS _{1_n} and CKE ₀ / CKE ₁ | CI2 | Min | 0.5 | pF | 1,2,4 |
| | | Max | 2.1 | pF | 1,2,4 |
| C _{delta} , all other input-only pins except CS _n and CKE | CDI1 | Min | -0.5 | pF | 1,2,5 |
| | | Max | 0.5 | pF | 1,2,5 |
| C _{delta} , CS _{0_n} / CS _{1_n} and CKE ₀ / CKE ₁ | CDI2 | Min | -0.5 | pF | 1,2,5,10 |
| | | Max | 0.5 | pF | 1,2,5,10 |
| Input/output capacitance, DQ, DM, DQS _t , DQS _c | CIO | Min | 2.0 | pF | 1,2,6,7 |
| | | Max | 4.8 | pF | 1,2,6,7 |
| Input/output capacitance delta, DQS _t , DQS _c | CDDQS | Min | 0.0 | pF | 1,2,7,8 |
| | | Max | 0.4 | pF | 1,2,7,8 |
| Input/output capacitance delta, DQ, DM | CDIO | Min | -0.5 | pF | 1,2,7,9 |
| | | Max | 0.5 | pF | 1,2,7,9 |
| Input/output capacitance ZQ Pin | CZQ | Min | 0.0 | pF | 1,2 |
| | | Max | 5.2 | pF | 1,2 |

(T_{OPER}; V_{DDQ} = 1.14~1.3V; V_{DDCA} = 1.14~1.3V; V_{DD1} = 1.7-1.95V, V_{DD2} = 1.14-1.3V)

NOTE :

- 1) This parameter applies to both die and package.
- 2) This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with VDD1, VDD2, VDDQ, VSS, VSSCA, VSSQ applied and all other pins floating.
- 3) Absolute value of C_{CK_t} - C_{CK_c}.
- 4) CI applies to CS_n, CKE, CA0-CA9, ODT.
- 5) C_{DI} = C_I - 0.5 × (C_{CK_t} - C_{CK_c})
- 6) DM loading matches DQ and DQS.
- 7) MR3 I/O configuration DS OP3-OP0 = 0001_B (34.3 Ω typical)
- 8) Absolute value of C_{DQS_t} and C_{DQS_c}.
- 9) C_{DIO} = C_{IO} - 0.5 × (C_{DQS_t} + C_{DQS_c}) in byte-lane.
- 10) C_{DI2} = C_{I2} - 0.25 × (C_{CK_t} + C_{CK_c})

15.0 IDD SPECIFICATION PARAMETERS AND TEST CONDITIONS

15.1 IDD Measurement Conditions

The following definitions are used within the IDD measurement tables unless stated otherwise:

LOW: $V_{IN} \leq V_{IL}(DC)$ MAX

HIGH: $V_{IN} \geq V_{IH}(DC)$ MIN

STABLE: Inputs are stable at a HIGH or LOW level

SWITCHING: See Table 37 and Table 38.

[Table 37] Definition of Switching for CA Input Signals

| Switching for CA | | | | | | | | |
|------------------|---|---|---|---|---|---|---|---|
| | CK_t (RISING) / CK_c (FALLING) | CK_t (FALLING) / CK_c (RISING) | CK_t (RISING) / CK_c (FALLING) | CK_t (FALLING) / CK_c (RISING) | CK_t (RISING) / CK_c (FALLING) | CK_t (FALLING) / CK_c (RISING) | CK_t (RISING) / CK_c (FALLING) | CK_t (FALLING) / CK_c (RISING) |
| Cycle | N | | N+1 | | N+2 | | N+3 | |
| CS_n | HIGH | | HIGH | | HIGH | | HIGH | |
| CA0 | HIGH | LOW | LOW | LOW | LOW | HIGH | HIGH | HIGH |
| CA1 | HIGH | HIGH | HIGH | LOW | LOW | LOW | LOW | HIGH |
| CA2 | HIGH | LOW | LOW | LOW | LOW | HIGH | HIGH | HIGH |
| CA3 | HIGH | HIGH | HIGH | LOW | LOW | LOW | LOW | HIGH |
| CA4 | HIGH | LOW | LOW | LOW | LOW | HIGH | HIGH | HIGH |
| CA5 | HIGH | HIGH | HIGH | LOW | LOW | LOW | LOW | HIGH |
| CA6 | HIGH | LOW | LOW | LOW | LOW | HIGH | HIGH | HIGH |
| CA7 | HIGH | HIGH | HIGH | LOW | LOW | LOW | LOW | HIGH |
| CA8 | HIGH | LOW | LOW | LOW | LOW | HIGH | HIGH | HIGH |
| CA9 | HIGH | HIGH | HIGH | LOW | LOW | LOW | LOW | HIGH |

NOTE :

1) CS_n must always be driven HIGH.

2) 50% of CA bus is changing between HIGH and LOW once per clock for the CA bus.

3) The above pattern (N, N+1, N+2, N+3...) is used continuously during IDD measurement for IDD values that require switching on the CA bus.

[Table 38] Definition of Switching for IDD4R

| Clock | CKE | CS_n | Clock Cycle Number | Command | CA[0:2] | CA[3:9] | All DQ |
|---------|-----|------|--------------------|--------------|---------|---------|--------|
| Rising | H | L | N | Read_Rising | HLH | LHLHLHL | L |
| Falling | H | L | N | Read_Falling | LLL | LLLLLLL | L |
| Rising | H | H | N + 1 | NOP | LLL | LLLLLLL | H |
| Falling | H | H | N + 1 | NOP | LLL | LLLLLLL | L |
| Rising | H | H | N + 2 | NOP | LLL | LLLLLLL | H |
| Falling | H | H | N + 2 | NOP | LLL | LLLLLLL | H |
| Rising | H | H | N + 3 | NOP | LLL | LLLLLLL | H |
| Falling | H | H | N + 3 | NOP | HLH | HLHLHL | L |
| Rising | H | L | N + 4 | Read_Rising | HLH | HLHLHL | H |
| Falling | H | L | N + 4 | Read_Falling | LHH | HHHHHHH | H |
| Rising | H | H | N + 5 | NOP | HHH | HHHHHHH | H |
| Falling | H | H | N + 5 | NOP | HHH | HHHHHHH | L |
| Rising | H | H | N + 6 | NOP | HHH | HHHHHHH | L |
| Falling | H | H | N + 6 | NOP | HHH | HHHHHHH | L |
| Rising | H | H | N + 7 | NOP | HHH | HHHHHHH | H |
| Falling | H | H | N + 7 | NOP | HLH | LHLHLHL | L |

NOTE :

- 1) Data strobe (DQS) is changing between HIGH and LOW every clock cycle.
 2) The above pattern (N, N+1...) is used continuously during IDD measurement for IDD4R.

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[Table 39] Definition of Switching for IDD4W

| Clock | CKE | CS_n | Clock Cycle Number | Command | CA[0:2] | CA[3:9] | All DQ |
|---------|-----|------|--------------------|---------------|---------|---------|--------|
| Rising | H | L | N | Write_Rising | HLL | LHLHLHL | L |
| Falling | H | L | N | Write_Falling | LLL | LLLLLLL | L |
| Rising | H | H | N + 1 | NOP | LLL | LLLLLLL | H |
| Falling | H | H | N + 1 | NOP | LLL | LLLLLLL | L |
| Rising | H | H | N + 2 | NOP | LLL | LLLLLLL | H |
| Falling | H | H | N + 2 | NOP | LLL | LLLLLLL | H |
| Rising | H | H | N + 3 | NOP | LLL | LLLLLLL | H |
| Falling | H | H | N + 3 | NOP | HLL | HLHLHL | L |
| Rising | H | L | N + 4 | Write_Rising | HLL | HLHLHL | H |
| Falling | H | L | N + 4 | Write_Falling | LHH | HHHHHHH | H |
| Rising | H | H | N + 5 | NOP | HHH | HHHHHHH | H |
| Falling | H | H | N + 5 | NOP | HHH | HHHHHHH | L |
| Rising | H | H | N + 6 | NOP | HHH | HHHHHHH | L |
| Falling | H | H | N + 6 | NOP | HHH | HHHHHHH | L |
| Rising | H | H | N + 7 | NOP | HHH | HHHHHHH | H |
| Falling | H | H | N + 7 | NOP | HLL | LHLHLHL | L |

NOTE :

1) Data strobe (DQS) is changing between HIGH and LOW every clock cycle.

2) Data masking (DM) must always be driven LOW.

3) The above pattern (N, N+1...) is used continuously during IDD measurement for IDD4W.

15.2 IDD Specifications

IDD values are for the entire operating voltage range, and all of them are for the entire standard range, with the exception of IDD6ET which is for the entire extended temperature range.

[Table 40] LPDDR3 IDD Specification Parameters and Operating Conditions

| Parameter/Condition | Symbol | Power Supply | Notes |
|--|----------------------|----------------|-------|
| Operating one bank active-precharge current: $t_{CK} = t_{CKmin}$; $t_{RC} = t_{RCmin}$; CKE is HIGH; CS_n is HIGH between valid commands; CA bus inputs are switching; Data bus inputs are stable ODT disabled | IDD0 ₁ | VDD1 | 12 |
| | IDD0 ₂ | VDD2 | 12 |
| | IDD0 _{in} | VDDCA, VDDQ | 3,12 |
| Idle power-down standby current: $t_{CK} = t_{CKmin}$; CKE is LOW; CS_n is HIGH; All banks are idle; CA bus inputs are switching; Data bus inputs are stable ODT disabled | IDD2P ₁ | VDD1 | 11 |
| | IDD2P ₂ | VDD2 | 11 |
| | IDD2P _{in} | VDDCA, VDDQ | 3,11 |
| Idle power-down standby current with clock stop: CK_t = LOW, CK_c = HIGH; CKE is LOW; CS_n is HIGH; All banks are idle; CA bus inputs are stable; Data bus inputs are stable ODT disabled | IDD2PS ₁ | VDD1 | 11 |
| | IDD2PS ₂ | VDD2 | 11 |
| | IDD2PS _{in} | VDDCA, VDDQ | 3,11 |

| Parameter/Condition | Symbol | Power Supply | Notes |
|---|----------------------|----------------|-------|
| Idle non power-down standby current: $t_{CK} = t_{CKmin}$; CKE is HIGH; CS_n is HIGH; All banks are idle; CA bus inputs are switching; Data bus inputs are stable ODT disabled | IDD2N ₁ | VDD1 | 12 |
| | IDD2N ₂ | VDD2 | 12 |
| | IDD2N _{in} | VDDCA, VDDQ | 3,12 |
| Idle non power-down standby current with clock stopped: CK_t=LOW; CK_c=HIGH; CKE is HIGH; CS_n is HIGH; All banks are idle; CA bus inputs are stable; Data bus inputs are stable ODT disabled | IDD2NS ₁ | VDD1 | 12 |
| | IDD2NS ₂ | VDD2 | 12 |
| | IDD2NS _{in} | VDDCA, VDDQ | 3,12 |
| Active power-down standby current: $t_{CK} = t_{CKmin}$; CKE is LOW; CS_n is HIGH; One bank is active; CA bus inputs are switching; Data bus inputs are stable ODT disabled | IDD3P ₁ | VDD1 | 12 |
| | IDD3P ₂ | VDD2 | 12 |
| | IDD3P _{in} | VDDCA, VDDQ | 3,12 |
| Active power-down standby current with clock stop: CK_t=LOW; CK_c=HIGH; CKE is LOW; CS_n is HIGH; One bank is active; CA bus inputs are stable; Data bus inputs are stable ODT disabled | IDD3PS ₁ | VDD1 | 12 |
| | IDD3PS ₂ | VDD2 | 12 |
| | IDD3PS _{in} | VDDCA, VDDQ | 4,12 |
| Active non-power-down standby current: $t_{CK} = t_{CKmin}$; CKE is HIGH; CS_n is HIGH; One bank is active; CA bus inputs are switching; Data bus inputs are stable ODT disabled | IDD3N ₁ | VDD1 | 12 |
| | IDD3N ₂ | VDD2 | 12 |
| | IDD3N _{in} | VDDCA, VDDQ | 4,12 |
| Active non-power-down standby current with clock stopped: CK_t=LOW; CK_c=HIGH; CKE is HIGH; CS_n is HIGH; One bank is active; CA bus inputs are stable; Data bus inputs are stable ODT disabled | IDD3NS ₁ | VDD1 | 12 |
| | IDD3NS ₂ | VDD2 | 12 |
| | IDD3NS _{in} | VDDCA, VDDQ | 4,12 |
| Operating burst READ current: $t_{CK} = t_{CKmin}$; CS_n is HIGH between valid commands; One bank is active; BL = 8; RL = RL(MIN); CA bus inputs are switching; 50% data change each burst transfer ODT disabled | IDD4R ₁ | VDD1 | 12 |
| | IDD4R ₂ | VDD2 | 12 |
| | IDD4R _{in} | VDDCA | 12 |
| | IDD4R _Q | VDDQ | 5,12 |
| Operating burst WRITE current: $t_{CK} = t_{CKmin}$; CS_n is HIGH between valid commands; One bank is active; BL = 8; WL = WLmin; CA bus inputs are switching; 50% data change each burst transfer ODT disabled | IDD4W ₁ | VDD1 | 12 |
| | IDD4W ₂ | VDD2 | 2 |
| | IDD4W _{in} | VDDCA, VDDQ | 4,12 |

| Parameter/Condition | Symbol | Power Supply | Notes |
|---|----------------------|----------------|---------------|
| All-bank REFRESH Burst current: $t_{CK} = t_{CKmin}$; CKE is HIGH between valid commands; $t_{RC} = t_{RFCabmin}$; Burst refresh; CA bus inputs are switching; Data bus inputs are stable; ODT disabled | IDD5 ₁ | VDD1 | 12 |
| | IDD5 ₂ | VDD2 | 12 |
| | IDD5 _{in} | VDDCA, VDDQ | 4, 12 |
| All-bank REFRESH Average current: $t_{CK} = t_{CKmin}$; CKE is HIGH between valid commands; $t_{RC} = t_{REFI}$; CA bus inputs are switching; Data bus inputs are stable; ODT disabled | IDD5AB ₁ | VDD1 | 12 |
| | IDD5AB ₂ | VDD2 | 12 |
| | IDD5AB _{in} | VDDCA, VDDQ | 4, 12 |
| Per-bank REFRESH Average current: $t_{CK} = t_{CKmin}$; CKE is HIGH between valid commands; $t_{RC} = t_{REFI}/8$; CA bus inputs are switching; Data bus inputs are stable; ODT disabled | IDD5PB ₁ | VDD1 | 12 |
| | IDD5PB ₂ | VDD2 | 12 |
| | IDD5PB _{in} | VDDCA, VDDQ | 4, 12 |
| Self refresh current (-25°C to +85°C): CK _t =LOW, CK _c =HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable; Maximum 1x Self-Refresh Rate; ODT disabled | IDD6 ₁ | VDD1 | 6,7,8,10,11 |
| | IDD6 ₂ | VDD2 | 6,7,8,10,11 |
| | IDD6 _{in} | VDDCA, VDDQ | 4,5,7,8,10,11 |

- NOTE :**
- 1) Published IDD values are the maximum of the distribution of the arithmetic mean.
 - 2) ODT disabled: MR11[2:0] = 000B.
 - 3) IDD current specifications are tested after the device is properly initialized.
 - 4) Measured currents are the summation of VDDQ and VDDCA.
 - 5) Guaranteed by design with output load of 5pF and RON = 40Ohm.
 - 6) The 1x Self-Refresh Rate is the rate at which the LPDDR3 device is refreshed internally during Self-Refresh, before going into the elevated Temperature range.
 - 7) This is the general definition that applies to full array Self Refresh. Refer to Table 42, IDD6 Partial Array Self-Refresh Current for details of Partial Array Self Refresh IDD6 specification.
 - 8) Supplier data sheets may contain additional Self Refresh IDD values for temperature subranges within the Standard or elevated Temperature Ranges.
 - 9) For all IDD measurements, VIHCKE = 0.8 × VDDCA, VILCKE = 0.2 × VDDCA.
 - 10) IDD6 85°C is guaranteed, IDD6 45°C is typical values.
 - 11) These specification values are under same condition of the both chips selected at the same time.
 - 12) These specification values are under IDD2PS condition of the other unselected chip

15.3 IDD Spec Table

[Table 41] IDD Specification for 8Gb DDP LPDDR3

| Symbol | | Power Supply | 128M x32 + 128M x32 | | Units |
|--------|----------------------|----------------|---------------------|----------|-------|
| | | | 1866Mbps | 1600Mbps | |
| IDD0 | IDD0 ₁ | VDD1 | 8.5 | 8.5 | mA |
| | IDD0 ₂ | VDD2 | 54.5 | 51.5 | mA |
| | IDD0 _{IN} | VDDCA, VDDQ | 0.2 | 0.2 | mA |
| IDD2P | IDD2P ₁ | VDD1 | 1 | | mA |
| | IDD2P ₂ | VDD2 | 3 | | mA |
| | IDD2P _{IN} | VDDCA, VDDQ | 0.2 | | mA |
| IDD2PS | IDD2PS ₁ | VDD1 | 1 | | mA |
| | IDD2PS ₂ | VDD2 | 3 | | mA |
| | IDD2PS _{IN} | VDDCA, VDDQ | 0.2 | | mA |
| IDD2N | IDD2N ₁ | VDD1 | 1.5 | 1.5 | mA |
| | IDD2N ₂ | VDD2 | 16.5 | 13.5 | mA |
| | IDD2N _{IN} | VDDCA, VDDQ | 0.2 | 0.2 | mA |
| IDD2NS | IDD2NS ₁ | VDD1 | 1.5 | 1.5 | mA |
| | IDD2NS ₂ | VDD2 | 13.5 | 11.5 | mA |
| | IDD2NS _{IN} | VDDCA, VDDQ | 0.2 | 0.2 | mA |
| IDD3P | IDD3P ₁ | VDD1 | 2.5 | 2.5 | mA |
| | IDD3P ₂ | VDD2 | 7.5 | 7.5 | mA |
| | IDD3P _{IN} | VDDCA, VDDQ | 0.2 | 0.2 | mA |
| IDD3PS | IDD3PS ₁ | VDD1 | 2.5 | 2.5 | mA |
| | IDD3PS ₂ | VDD2 | 7.5 | 7.5 | mA |
| | IDD3PS _{IN} | VDDCA, VDDQ | 0.2 | 0.2 | mA |
| IDD3N | IDD3N ₁ | VDD1 | 2.5 | 2.5 | mA |
| | IDD3N ₂ | VDD2 | 19.5 | 16.5 | mA |
| | IDD3N _{IN} | VDDCA, VDDQ | 0.2 | 0.2 | mA |
| IDD3NS | IDD3NS ₁ | VDD1 | 2.5 | 2.5 | mA |
| | IDD3NS ₂ | VDD2 | 16.5 | 14.5 | mA |
| | IDD3NS _{IN} | VDDCA, VDDQ | 0.2 | 0.2 | mA |
| IDD4R | IDD4R ₁ | VDD1 | 2.5 | 2.5 | mA |
| | IDD4R ₂ | VDD2 | 211.5 | 181.5 | mA |
| | IDD4R _{IN} | VDDCA | 0.15 | 0.15 | mA |
| | IDD4R _Q | VDDQ | 260.05 | 220.05 | mA |
| IDD4W | IDD4W ₁ | VDD1 | 2.5 | 2.5 | mA |
| | IDD4W ₂ | VDD2 | 141.5 | 121.5 | mA |
| | IDD4W _{IN} | VDDCA, VDDQ | 45.1 | 40.1 | mA |

| Symbol | | | Power Supply | 128M x32 + 128M x32 | | Units |
|--------|----------------------|------|--------------|---------------------|----------|-------|
| | | | | 1866Mbps | 1600Mbps | |
| IDD5 | IDD5 ₁ | | VDD1 | 37.5 | 37.5 | mA |
| | IDD5 ₂ | | VDD2 | 176.5 | 166.5 | mA |
| | IDD5 _{IN} | | VDDCA, VDDQ | 0.2 | 0.2 | mA |
| IDD5AB | IDD5AB ₁ | | VDD1 | 3.5 | 3.5 | mA |
| | IDD5AB ₂ | | VDD2 | 22.5 | 19.5 | mA |
| | IDD5AB _{IN} | | VDDCA, VDDQ | 0.2 | 0.2 | mA |
| IDD5PB | IDD5PB ₁ | | VDD1 | 3.5 | 3.5 | mA |
| | IDD5PB ₂ | | VDD2 | 24.5 | 21.5 | mA |
| | IDD5PB _{IN} | | VDDCA, VDDQ | 0.2 | 0.2 | mA |
| IDD6 | IDD6 ₁ | 45°C | VDD1 | 0.36 | | mA |
| | | 85°C | | 2.8 | | |
| | IDD6 ₂ | 45°C | VDD2 | 1.6 | | mA |
| | | 85°C | | 10.4 | | |
| | IDD6 _{IN} | 45°C | VDDCA, VDDQ | 0.04 | | mA |
| | | 85°C | | 0.2 | | |

NOTE :

1) See Table 40, LPDDR3 IDD Specification Parameters and Operating Conditions for notes.

[Table 42] IDD6 Partial Array Self-Refresh Current

| Parameter | | | 8Gb DDP | | Unit |
|---|------------|--------------|---------|-------|------|
| | | | 45°C | 85°C | |
| IDD6 Partial Array Self-Refresh Current (max) | Full Array | VDD1 | 360 | 2800 | uA |
| | | VDD2 | 1600 | 10400 | |
| | | VDDCA , VDDQ | 40 | 200 | |
| | 1/2 Array | VDD1 | 320 | 2000 | uA |
| | | VDD2 | 1120 | 6800 | |
| | | VDDCA , VDDQ | 40 | 200 | |
| | 1/4 Array | VDD1 | 280 | 1600 | uA |
| | | VDD2 | 760 | 5000 | |
| | | VDDCA , VDDQ | 40 | 200 | |
| | 1/8 Array | VDD1 | 240 | 1400 | uA |
| | | VDD2 | 600 | 4000 | |
| | | VDDCA , VDDQ | 40 | 200 | |

NOTE :

1) PASR(Partial Array Self-Refresh) function will be supported upon request. Please contact Samsung for more information.

16.0 ELECTRICAL CHARACTERISTICS AND AC TIMING

16.1 Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the LPDDR3 device.

16.1.1 Definition for $t_{CK}(avg)$ and n_{CK}

$t_{CK}(avg)$ is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$t_{CK}(avg) = \left(\sum_{j=1}^N t_{CK_j} \right) / N$$

where $N = 200$

Unit ' $t_{CK}(avg)$ ' represents the actual clock average $t_{CK}(avg)$ of the input clock under operation. Unit ' n_{CK} ' represents one clock cycle of the input clock, counting the actual clock edges.

$t_{CK}(avg)$ may change by up to +/-1% within a 100 clock cycle window, provided that all jitter and timing specs are met.

16.1.2 Definition for $t_{CK}(abs)$

$t_{CK}(abs)$ is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge.

$t_{CK}(abs)$ is not subject to production test.

16.1.3 Definition for $t_{CH}(avg)$ and $t_{CL}(avg)$

$t_{CH}(avg)$ is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$t_{CH}(avg) = \left(\sum_{j=1}^N t_{CH_j} \right) / (N \times t_{CK}(avg))$$

where $N = 200$

$t_{CL}(avg)$ is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$t_{CL}(avg) = \left(\sum_{j=1}^N t_{CL_j} \right) / (N \times t_{CK}(avg))$$

where $N = 200$

16.1.4 Definition for $t_{JIT}(per)$

$t_{JIT}(per)$ is the single period jitter defined as the largest deviation of any signal t_{CK} from $t_{CK}(avg)$.

$t_{JIT}(per) = \text{Min/max of } \{t_{CK_i} - t_{CK}(avg) \text{ where } i = 1 \text{ to } 200\}.$

$t_{JIT}(per)_{act}$ is the actual clock jitter for a given system.

$t_{JIT}(per)_{allowed}$ is the specified allowed clock period jitter.

$t_{JIT}(per)$ is not subject to production test.

16.1.5 Definition for $t_{JIT(cc)}$

$t_{JIT(cc)}$ is defined as the absolute difference in clock period between two consecutive clock cycles.

$t_{JIT(cc)} = \text{Max of } \{t_{CK_{i+1}} - t_{CK_i}\}$.

$t_{JIT(cc)}$ defines the cycle to cycle jitter.

$t_{JIT(cc)}$ is not subject to production test.

16.1.6 Definition for $t_{ERR(nper)}$

$t_{ERR(nper)}$ is defined as the cumulative error across n multiple consecutive cycles from $t_{CK(avg)}$.

$t_{ERR(nper),act}$ is the actual clock jitter over n cycles for a given system.

$t_{ERR(nper),allowed}$ is the specified allowed clock period jitter over n cycles.

$t_{ERR(nper)}$ is not subject to production test.

$$t_{ERR(nper)} = \left(\sum_{j=i}^{i+n-1} t_{CK_j} \right) - n \times t_{CK(avg)}$$

$t_{ERR(nper),min}$ can be calculated by the formula shown below:

$$t_{ERR(nper),min} = (1 + 0.68LN(n)) \times t_{JIT(per),min}$$

$t_{ERR(nper),max}$ can be calculated by the formula shown below

$$t_{ERR(nper),max} = (1 + 0.68LN(n)) \times t_{JIT(per),max}$$

Using these equations, $t_{ERR(nper)}$ tables can be generated for each $t_{JIT(per),act}$ value.

16.1.7 Definition for duty cycle jitter $t_{JIT(duty)}$

$t_{JIT(duty)}$ is defined with absolute and average specification of t_{CH} / t_{CL} .

$$t_{JIT(duty),min} = \text{MIN}((t_{CH(abs),min} - t_{CH(avg),min}), (t_{CL(abs),min} - t_{CL(avg),min})) \times t_{CK(avg)}$$

$$t_{JIT(duty),max} = \text{MAX}((t_{CH(abs),max} - t_{CH(avg),max}), (t_{CL(abs),max} - t_{CL(avg),max})) \times t_{CK(avg)}$$

16.1.8 Definition for $t_{CK(abs)}$, $t_{CH(abs)}$ and $t_{CL(abs)}$

These parameters are specified per their average values, however it is understood that the following relationship between the average timing and the absolute instantaneous timing holds at all times.

[Table 43] Definition for $t_{CK(abs)}$, $t_{CH(abs)}$, and $t_{CL(abs)}$

| Parameter | Symbol | Min | Unit |
|---------------------------------|---------------|---|---------------|
| Absolute Clock Period | $t_{CK(abs)}$ | $t_{CK(avg),min} + t_{JIT(per),min}$ | ps |
| Absolute Clock HIGH Pulse Width | $t_{CH(abs)}$ | $t_{CH(avg),min} + t_{JIT(duty),min} / t_{CK(avg),min}$ | $t_{CK(avg)}$ |
| Absolute Clock LOW Pulse Width | $t_{CL(abs)}$ | $t_{CL(avg),min} + t_{JIT(duty),min} / t_{CK(avg),min}$ | $t_{CK(avg)}$ |

NOTE :

1) $t_{CK(avg),min}$ is expressed in ps for this table.

2) $t_{JIT(duty),min}$ is a negative value.

16.2 Period Clock Jitter

LPDDR3 devices can tolerate some clock period jitter without core timing parameter de-rating. This section describes device timing requirements in the presence of clock period jitter (tJIT(per)) in excess of the values found in Table 46 and how to determine cycle time de-rating and clock cycle de-rating.

16.2.1 Clock period jitter effects on core timing parameters

(tRCD, tRP, tRTP, tWR, tWRA, tWTR, tRC, tRAS, tRRD, tFAW)

Core timing parameters extend across multiple clock cycles. Period clock jitter will impact these parameters when measured in numbers of clock cycles. When the device is operated with clock jitter within the specification limits, the LPDDR3 device is characterized and verified to support $tnPARAM = RU\{tPARAM / tCK(avg)\}$.

When the device is operated with clock jitter outside specification limits, the number of clocks or tCK(avg) may need to be increased based on the values for each core timing parameter.

16.2.1.1 Cycle time de-rating for core timing parameters

For a given number of clocks (tnPARAM), for each core timing parameter, average clock period (tCK(avg)) and actual cumulative period error (tERR(tnPARAM),act) in excess of the allowed cumulative period error (tERR(tnPARAM),allowed), the equation below calculates the amount of cycle time de-rating (in ns) required if the equation results in a positive value for a core timing parameter.

$$CycleTimeDerating = MAX\left\{\left(\frac{tPARAM + tERR(tnPARAM),act - tERR(tnPARAM),allowed}{tnPARAM} - tCK(avg)\right), 0\right\}$$

A cycle time derating analysis should be conducted for each core timing parameter. The amount of cycle time derating required is the maximum of the cycle time de-ratings determined for each individual core timing parameter.

16.2.1.2 Clock Cycle de-rating for core timing parameters

For a given number of clocks (tnPARAM) for each core timing parameter, clock cycle de-rating should be specified with amount of period jitter (tJIT(per)).

For a given number of clocks (tnPARAM), for each core timing parameter, average clock period (tCK(avg)) and actual cumulative period error (tERR(tnPARAM),act) in excess of the allowed cumulative period error (tERR(tnPARAM),allowed), the equation below calculates the clock cycle derating (in clocks) required if the equation results in a positive value for a core timing parameter.

$$ClockCycleDerating = RU\left\{\frac{tPARAM + tERR(tnPARAM),act - tERR(tnPARAM),allowed}{tCK(avg)}\right\} - tnPARAM$$

A clock cycle de-rating analysis should be conducted for each core timing parameter.

16.2.2 Clock jitter effects on Command/Address timing parameters

(tISCA, tIHCA, tISCS, tIHCS, tISCKE, tIHCKE, tISb, tIHb, tISCKEb, tIHCKEb)

These parameters are measured from a command/address signal (CKE, CS_n, CA0 - CA9) transition edge to its respective clock signal (CK_t/CK_c) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per)), as the setup and hold are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values shall be met.

16.2.3 Clock jitter effects on Read timing parameters

16.2.3.1 tRPRE

When the device is operated with input clock jitter, tRPRE needs to be de-rated by the actual period jitter (tJIT(per),act,max) of the input clock in excess of the allowed period jitter (tJIT(per),allowed,max). Output de-ratings are relative to the input clock.

$$tRPRE(min, derated) = 0.9 - \left(\frac{tJIT(per), act, max - tJIT(per), allowed, max}{tCK(avg)} \right)$$

For example,

if the measured jitter into a LPDDR3-1600 device has tCK(avg) = 1250 ps, tJIT(per),act,min = -92 ps and tJIT(per),act,max = + 134 ps, then tRPRE,min,derated = 0.9 - (tJIT(per),act,max - tJIT(per),allowed,max)/tCK(avg) = 0.9 - (134 - 100)/1250 = .8728 tCK(avg)

16.2.3.2 tLZ(DQ), tHZ(DQ), tDQSCK, tLZ(DQS), tHZ(DQS)

These parameters are measured from a specific clock edge to a data signal (DMn, DQm.: n=0,1,2,3. m=0 –31) transition and will be met with respect to that clock edge. Therefore, they are not affected by the amount of clock jitter applied (i.e. tJIT(per)).

16.2.3.3 tQSH, tQSL

These parameters are affected by duty cycle jitter which is represented by tCH(abs)min and tCL(abs)min.

These parameters determine absolute Data-Valid window(DVW) at the LPDDR3 device pin.

Absolute min DVW @LPDDR3 device pin =

min { (tQSH(abs)min – tDQSQmax), (tQSL(abs)min – tDQSQmax) }

This minimum DVW shall be met at the target frequency regardless of clock jitter.

16.2.3.4 tRPST

tRPST is affected by duty cycle jitter which is represented by tCL(abs). Therefore tRPST(abs)min can be specified by tCL(abs)min.

tRPST(abs)min = tCL(abs)min – 0.05 = tQSL(abs)min

16.2.4 Clock jitter effects on Write timing parameters

16.2.4.1 tDS, tDH

These parameters are measured from a data signal (DMn, DQm.: n=0,1,2,3. m=0 –31) transition edge to its respective data strobe signal (DQSn, \overline{DQSn} : n=0,1,2,3) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per)), as the setup and hold are relative to the data strobe signal crossing that latches the data. Regardless of clock jitter values, these values shall be met.

16.2.4.2 tDSS, tDSH

These parameters are measured from a data strobe signal (DQSx_t, DQSx_c) crossing to its respective clock signal (CK_t/CK_c) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per)), as the setup and hold of the data strobes are relative to the corresponding clock signal crossing. Regardless of clock jitter values, these values shall be met.

16.2.4.3 tDQSS

This parameter is measured from a data strobe signal (DQSx_t, DQSx_c) crossing to the subsequent clock signal (CK_t/CK_c) crossing. When the device is operated with input clock jitter, this parameter needs to be de-rated by the actual period jitter tJIT(per),act of the input clock in excess of the allowed period jitter tJIT(per),allowed.

$$tDQSS(min, derated) = 0.75 - \frac{tJIT(per), act, min - tJIT(per), allowed, min}{tCK(avg)}$$

$$tDQSS(max, derated) = 1.25 - \frac{tJIT(per), act, max - tJIT(per), allowed, max}{tCK(avg)}$$

For example,

if the measured jitter into a LPDDR3-1600 device has tCK(avg)= 1250 ps, tJIT(per),act,min = -93 ps and tJIT(per),act,max= + 134 ps, then

tDQSS,(min,derated) = 0.75 - (tJIT(per),act,min - tJIT(per),allowed,min)/tCK(avg) = 0.75 - (-93 + 100)/1250 = 0.7444 tCK(avg)

and

tDQSS,(max,derated) = 1.25 - (tJIT(per),act,max - tJIT(per),allowed,max)/tCK(avg) = 1.25 - (134 - 100)/1250 = 1.2228 tCK(avg)

16.3 LPDDR3 Refresh Requirements by Device Density

[Table 44] LPDDR3 Refresh Requirement Parameters (per density)

| Parameter | | Symbol | 4 Gb | Unit |
|--|-------|---------------------|--------|------|
| Number of Banks | | | 8 | |
| Refresh Window Tcase ≤ 85°C | | t _{REFW} | 32 | ms |
| Refresh Window 1/2-Rate Refresh | | t _{REFW} | 16 | ms |
| Refresh Window 1/4-Rate Refresh | | t _{REFW} | 8 | ms |
| Required number of REFRESH commands (min) | | R | 8,192 | - |
| average time between REFRESH commands (for reference only) Tcase ≤ 85°C | REFab | t _{REFI} | 3.9 | us |
| | REFpb | t _{REFIpb} | 0.4875 | us |
| Refresh Cycle time | | t _{RFCab} | 130 | ns |
| Per Bank Refresh Cycle time | | t _{RFCpb} | 60 | ns |

NOTE :

1) Please refer to LPDDR3 SDRAM Addressing.

[Table 45] LPDDR3 Read and Write Latencies

| Parameter | Value | | Unit |
|-------------------------------------|-------|-------|----------|
| | 1600 | 1866 | |
| Max. Clock frequency | 800 | 933 | MHz |
| Max. Data Rate | 1600 | 1866 | MT/s |
| Average Clock Period | 1.25 | 1.071 | ns |
| Read Latency | 12 | 14 | tCK(avg) |
| Write Latency (Set A) | 6 | 8 | tCK(avg) |
| Write Latency (Set B) ¹⁾ | 9 | 11 | tCK(avg) |

NOTE:

1) Write Latency (Set B) support is an optional feature. Refer to MR0 OP<6>.

16.4 AC Timing

Notes 1), 2), 3) and 4) apply to all parameters.

[Table 46] LPDDR3 AC Timing Table

| Parameter | Symbol | Min/Max | Data Rate | | Unit |
|---|---------------------------|---------|---|------|---------------|
| | | | 1866 | 1600 | |
| Maximum clock frequency | f_{CK} | - | 933 | 800 | MHz |
| Clock Timing | | | | | |
| Average Clock Period | $t_{CK(avg)}$ | MIN | 1.071 | 1.25 | ns |
| | | MAX | 100 | | |
| Average HIGH pulse width | $t_{CH(avg)}$ | MIN | 0.45 | | $t_{CK(avg)}$ |
| | | MAX | 0.55 | | |
| Average LOW pulse width | $t_{CL(avg)}$ | MIN | 0.45 | | $t_{CK(avg)}$ |
| | | MAX | 0.55 | | |
| Absolute clock period | $t_{CK(abs)}$ | MIN | $t_{CK(avg)} \text{ MIN} + t_{JIT(per)} \text{ MIN}$ | | ns |
| Absolute clock HIGH pulse width | $t_{CH(abs)}$ | MIN | 0.43 | | $t_{CK(avg)}$ |
| | | MAX | 0.57 | | |
| Absolute clock LOW pulse width | $t_{CL(abs)}$ | MIN | 0.43 | | $t_{CK(avg)}$ |
| | | MAX | 0.57 | | |
| Clock period jitter (with supported jitter) | $t_{JIT(per), allowed}$ | MIN | -60 | -70 | ps |
| | | MAX | 60 | 70 | |
| Maximum Clock Jitter between two consecutive clock cycles (with allowed jitter) | $t_{JIT(cc), allowed}$ | MAX | 120 | 140 | ps |
| Duty cycle jitter (with supported jitter) | $t_{JIT(duty), allowed}$ | MIN | $\min((t_{CH(abs),min} - t_{CH(avg),min}), (t_{CL(abs),min} - t_{CL(avg),min})) \times t_{CK(avg)}$ | | ps |
| | | MAX | $\max((t_{CH(abs),max} - t_{CH(avg),max}), (t_{CL(abs),max} - t_{CL(avg),max})) \times t_{CK(avg)}$ | | |
| Cumulative error across 2 cycles | $t_{ERR(2per), allowed}$ | MIN | -88 | -103 | ps |
| | | MAX | 88 | 103 | |
| Cumulative error across 3 cycles | $t_{ERR(3per), allowed}$ | MIN | -105 | -122 | ps |
| | | MAX | 105 | 122 | |
| Cumulative error across 4 cycles | $t_{ERR(4per), allowed}$ | MIN | -117 | -136 | ps |
| | | MAX | 117 | 136 | |
| Cumulative error across 5 cycles | $t_{ERR(5per), allowed}$ | MIN | -126 | -147 | ps |
| | | MAX | 126 | 147 | |
| Cumulative error across 6 cycles | $t_{ERR(6per), allowed}$ | MIN | -133 | -155 | ps |
| | | MAX | 133 | 155 | |
| Cumulative error across 7 cycles | $t_{ERR(7per), allowed}$ | MIN | -139 | -163 | ps |
| | | MAX | 139 | 163 | |
| Cumulative error across 8 cycles | $t_{ERR(8per), allowed}$ | MIN | -145 | -169 | ps |
| | | MAX | 145 | 169 | |
| Cumulative error across 9 cycles | $t_{ERR(9per), allowed}$ | MIN | -150 | -175 | ps |
| | | MAX | 150 | 175 | |
| Cumulative error across 10 cycles | $t_{ERR(10per), allowed}$ | MIN | -154 | -180 | ps |
| | | MAX | 154 | 180 | |
| Cumulative error across 11 cycles | $t_{ERR(11per), allowed}$ | MIN | -158 | -184 | ps |
| | | MAX | 158 | 184 | |
| Cumulative error across 12 cycles | $t_{ERR(12per), allowed}$ | MIN | -161 | -188 | ps |
| | | MAX | 161 | 188 | |

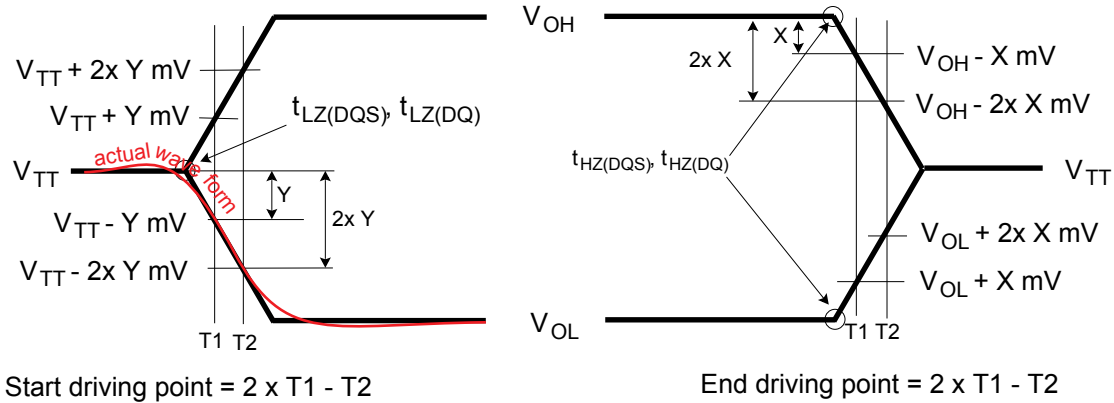
| Parameter | Symbol | Min/Max | Data Rate | | Unit |
|--|----------------------------|---------|---|------|----------------------|
| | | | 1866 | 1600 | |
| Cumulative error across n = 13, 14 . . . 19, 20 cycles | $t_{ERR(nper), allowed}$ | MIN | $t_{ERR(nper), allowed} MIN = (1 + 0.68ln(n)) \times t_{JIT(per), allowed} MIN$ | | ps |
| | | MAX | $t_{ERR(nper), allowed} MAX = (1 + 0.68ln(n)) \times t_{JIT(per), allowed} MAX$ | | |
| ZQ Calibration Parameters | | | | | |
| Initialization calibration time | t_{ZQINIT} | MIN | 1 | | us |
| Long calibration time | t_{ZQCL} | MIN | 360 | | ns |
| Short calibration time | t_{ZQCS} | MIN | 90 | | ns |
| Calibration RESET Time | $t_{ZQRESET}$ | MIN | Max (50ns, 3t _{CK}) | | ns |
| READ Parameters ⁴⁾ | | | | | |
| DQS output access time from CK_t/CK_c | t_{DQSK} | MIN | 2500 | | ps |
| | | MAX | 5500 | | |
| DQSCK delta short ⁵⁾ | t_{DQSKDS} | MAX | 190 | 220 | ps |
| DQSCK delta medium ⁶⁾ | t_{DQSKDM} | MAX | 435 | 511 | ps |
| DQSCK delta long ⁷⁾ | t_{DQSKDL} | MAX | 525 | 614 | ps |
| DQS - DQ skew | t_{DQSQ} | MAX | 115 | 135 | ps |
| DQS Output High Pulse Width | t_{QSH} | MIN | t _{CH(abs)} - 0.05 | | t _{CK(avg)} |
| DQS Output Low Pulse Width | t_{QSL} | MIN | t _{CL(abs)} - 0.05 | | t _{CK(avg)} |
| DQ / DQS output hold time from DQS | t_{QH} | MIN | min(t _{QSH} , t _{QSL}) | | ps |
| Read preamble ^{8), 11)} | t_{RPRE} | MIN | 0.9 | | t _{CK(avg)} |
| Read postamble ^{8), 12)} | t_{RPST} | MIN | 0.3 | | t _{CK(avg)} |
| DQS low-Z from clock ⁸⁾ | $t_{LZ(DQS)}$ | MIN | t _{DQSK(MIN)} - 300 | | ps |
| DQ low-Z from clock ⁸⁾ | $t_{LZ(DQ)}$ | MIN | t _{DQSK,(MIN)} - 300 | | ps |
| DQS high-Z from clock ⁸⁾ | $t_{HZ(DQS)}$ | MAX | t _{DQSK,(MAX)} - 100 | | ps |
| DQ high-Z from clock ⁸⁾ | $t_{HZ(DQ)}$ | MAX | t _{DQSK,(MAX)} + (1.4 × t _{DQSQ,(MAX)}) | | ps |
| WRITE Parameters ⁴⁾ | | | | | |
| DQ and DM input hold time (Vref based) | t_{DH} | MIN | 130 | 150 | ps |
| DQ and DM input setup time (Vref based) | t_{DS} | MIN | 130 | 150 | ps |
| DQ and DM input pulse width | t_{DIPW} | MIN | 0.35 | | t _{CK(avg)} |
| Write command to 1st DQS latching transition | t_{DQSS} | MIN | 0.75 | | t _{CK(avg)} |
| | | MAX | 1.25 | | |
| DQS input high-level width | t_{DQSH} | MIN | 0.4 | | t _{CK(avg)} |
| DQS input low-level width | t_{DQSL} | MIN | 0.4 | | t _{CK(avg)} |
| DQS falling edge to CK setup time | t_{DSS} | MIN | 0.2 | | t _{CK(avg)} |
| DQS falling edge hold time from CK | t_{DSH} | MIN | 0.2 | | t _{CK(avg)} |
| Write postamble | t_{WPST} | MIN | 0.4 | | t _{CK(avg)} |
| Write preamble | t_{WPRE} | MIN | 0.8 | | t _{CK(avg)} |
| CKE Input Parameters | | | | | |
| CKE minimum pulse width (HIGH and LOW pulse width) | t_{CKE} | MIN | max(7.5ns, 3t _{CK}) | | ns |
| CKE input setup time | t_{ISCKE} ¹³⁾ | MIN | 0.25 | | t _{CK(avg)} |
| CKE input hold time | t_{IHCKE} ¹⁴⁾ | MIN | 0.25 | | t _{CK(avg)} |
| Command path disable delay | t_{CPDED} | MIN | 2 | | t _{CK(avg)} |
| Command Address Input Parameters ⁴⁾ | | | | | |
| Address and control input setup time | t_{ISCA} ¹⁵⁾ | MIN | 130 | 150 | ps |
| Address and control input hold time | t_{IHCA} ¹⁵⁾ | MIN | 130 | 150 | ps |

| Parameter | Symbol | Min/Max | Data Rate | | Unit |
|--|----------------------------------|---------|--|------|----------------------|
| | | | 1866 | 1600 | |
| CS_n input setup time | t _{ISCS} ¹⁵⁾ | MIN | 230 | 270 | ps |
| CS_n input hold time | t _{IHCS} ¹⁵⁾ | MIN | 230 | 270 | ps |
| Address and control input pulse width | t _{IPWCA} | MIN | 0.35 | | t _{CK(avg)} |
| CS_n input pulse width | t _{IPWCS} | MIN | 0.7 | | t _{CK(avg)} |
| Boot Parameters (10 MHz - 55 MHz) ^{16), 17), 18)} | | | | | |
| Clock Cycle Time | t _{CKb} | MAX | 100 | | ns |
| | | MIN | 18 | | |
| CKE Input Setup Time | t _{ISCKEb} | MIN | 2.5 | | ns |
| CKE Input Hold Time | t _{IHCKEb} | MIN | 2.5 | | ns |
| Address and Control Input Setup Time | t _{ISb} | MIN | 1150 | | ps |
| Address and Control Input Hold Time | t _{IHb} | MIN | 1150 | | ps |
| DQS Output Data Access Time from CK_t/CK_c | t _{DQSCb} | MIN | 2.0 | | ns |
| | | MAX | 10.0 | | |
| Data Strobe Edge to Output Data Edge | t _{DQSQb} | MAX | 1.2 | | ns |
| Mode Register Parameters | | | | | |
| MODE REGISTER WRITE command period | t _{MRW} | MIN | 10 | | t _{CK(avg)} |
| MODE REGISTER READ command period | t _{MRR} | MIN | 4 | | t _{CK(avg)} |
| Mode register set command delay | t _{MRD} | MIN | Max(14ns, 10tCK) | | ns |
| Core Parameters ¹⁹⁾ | | | | | |
| READ latency | RL | MIN | 14 | 12 | t _{CK(avg)} |
| WRITE latency (set A) | WL | MIN | 8 | 6 | t _{CK(avg)} |
| WRITE latency (set B) | WL | MIN | 11 | 9 | t _{CK(avg)} |
| ACTIVATE-to-ACTIVATE command period | t _{RC} | MIN | t _{RAS} + t _{RPab} (with all-bank precharge) t _{RAS} + t _{RPpb} (with per-bank precharge) | | ns |
| CKE minimum pulse width during SELF REFRESH (low pulse width during SELF REFRESH) | t _{CKESR} | MIN | Max(15ns, 3t _{CK}) | | ns |
| SELF REFRESH exit to next valid command delay | t _{XSR} | MIN | Max (t _{RFCab} + 10ns, 2t _{CK}) | | ns |
| Exit power down to next valid command delay | t _{XP} | MIN | Max(7.5ns, 3t _{CK}) | | ns |
| CAS-to-CAS delay | t _{CCD} | MIN | 4 | | t _{CK(avg)} |
| Internal READ to PRECHARGE command delay | t _{RTP} | MIN | Max(7.5ns, 4t _{CK}) | | ns |
| RAS-to-CAS delay | t _{RCD(typ)} | MIN | Max (18ns, 3t _{CK}) | | ns |
| Row precharge Time (single bank) | t _{RPpb (typ)} | MIN | Max (18ns, 3t _{CK}) | | ns |
| Row Precharge Time (all banks) | t _{RPab (typ)} | MIN | Max(21ns, 3t _{CK}) | | ns |
| Row active time | t _{RAS} | MIN | Max(42ns, 3t _{CK}) | | ns |
| | | MAX | 70 | | us |
| WRITE recovery time | t _{WR} | MIN | Max(15ns, 4t _{CK}) | | ns |
| Internal WRITE-to-READ command delay | t _{WTR} | MIN | Max(7.5ns, 4t _{CK}) | | ns |
| Active bank A to Active bank B | t _{R RD} | MIN | Max(10ns, 2t _{CK}) | | ns |
| Four bank ACTIVATE Window | t _{FAW} | MIN | Max(50ns, 8t _{CK}) | | ns |
| ODT Parameters | | | | | |
| Asynchronous R _{TT} turn-on delay from ODT input | t _{ODTon} | MIN | 1.75 | | ns |
| | | MAX | 3.5 | | |
| Asynchronous R _{TT} turn-off delay from ODT input | t _{ODToff} | MIN | 1.75 | | ns |
| | | MAX | 3.5 | | |
| Automatic R _{TT} turn-on delay after READ data | t _{AODTon} | MAX | t _{DQSC} + 1.4 × t _{DQSQ,max} + t _{CK(avg,min)} | | ps |

| Parameter | Symbol | Min/Max | Data Rate | | Unit |
|--|----------------------|---------|--|------|----------------------|
| | | | 1866 | 1600 | |
| Automatic R _{TT} turn-off delay after READ data | t _{AODToff} | MIN | t _{DQSCK,min} - 300 | | ps |
| R _{TT} disable delay from power down, self refresh | t _{ODTd} | MAX | 12 | | ns |
| R _{TT} enable delay from power down and self refresh exit | t _{ODTe} | MAX | 12 | | ns |
| CA Training Parameters | | | | | |
| First CA calibration Command after CA calibration mode is programmed | t _{CAMRD} | MIN | 20 | | t _{CK(avg)} |
| First CA calibration Command after CKE is LOW | t _{CAENT} | MIN | 10 | | t _{CK(avg)} |
| CA calibration Exit Command after CKE is HIGH | t _{CAEXT} | MIN | 10 | | t _{CK(avg)} |
| CKE LOW after CA calibration mode is programmed | t _{CACKEL} | MIN | 10 | | t _{CK(avg)} |
| CKE HIGH after the last CA calibration results are driven. | t _{CACKEH} | MIN | 10 | | t _{CK(avg)} |
| Data out delay after CA training calibration command is programmed | t _{ADR} | MAX | 20 | | ns |
| MRW CA exit command to DQ tri-state | t _{MRZ} | MIN | 3 | | ns |
| CA calibration command to CA calibration command delay | t _{CACD} | MIN | RU(t _{ADR} +2 × t _{CK}) | | t _{CK(avg)} |
| Write Leveling Parameters | | | | | |
| DQS_t/DQS_c delay after write leveling mode is programmed | t _{WLDQSEN} | MIN | 25 | | ns |
| First DQS_t/DQS_c edge after write leveling mode is programmed | t _{WLMRD} | MIN | 40 | | ns |
| Write leveling output delay | t _{WLO} | MAX | 20 | | ns |
| Write leveling hold time | t _{WLH} | MIN | 150 | 175 | ps |
| Write leveling setup time | t _{WLS} | MIN | 150 | 175 | ps |
| Temperature De-Rating ¹⁸⁾ | | | | | |
| DQS output access time from CK_t/CK_c (derated) | t _{DQSCK} | MAX | 5620 | | ps |
| RAS-to-CAS delay (derated) | t _{RCD} | MIN | t _{RCD} + 1.875 | | ns |
| ACTIVATE-to- ACTIVATE command period (derated) | t _{RC} | MIN | t _{RAS} (derated) + t _{RP} (derated) | | ns |
| Row active time (derated) | t _{RAS} | MIN | t _{RAS} + 1.875 | | ns |
| Row precharge time (derated) | t _{RP} | MIN | t _{RP} + 1.875 | | ns |
| Active bank A to active bank B (derated) | t _{RRD} | MIN | t _{RRD} + 1.875 | | ns |

NOTE :

- 1) Frequency values are for reference only. Clock cycle time (tCK) is used to determine device capabilities.
- 2) All AC timings assume an input slew rate of 2 V/ns for single ended signals.
- 3) Measured with 4 V/ns differential CK_t/CK_c slew rate and nominal V_{IX}.
- 4) READ, WRITE, and Input setup and hold values are referenced to V_{REF}.
- 5) t_{DQSKCKDS} is the absolute value of the difference between any two t_{DQSKCK} measurements (in a byte lane) within a contiguous sequence of bursts in a 160ns rolling window. t_{DQSKCKDS} is not tested and is guaranteed by design. Temperature drift in the system is < 10°C/s. Values do not include clock jitter.
- 6) t_{DQSKCKDM} is the absolute value of the difference between any two t_{DQSKCK} measurements (in a byte lane) within a 1.6us rolling window. t_{DQSKCKDM} is not tested and is guaranteed by design. Temperature drift in the system is < 10°C/s. Values do not include clock jitter.
- 7) t_{DQSKCKDL} is the absolute value of the difference between any two t_{DQSKCK} measurements (in a byte lane) within a 32ms rolling window. t_{DQSKCKDL} is not tested and is guaranteed by design. Temperature drift in the system is < 10°C/s. Values do not include clock jitter.
- 8) For LOW-to-HIGH and HIGH-to-LOW transitions, the timing reference is at the point when the signal crosses the transition threshold (V_{TT}). tHZ and tLZ transitions occur in the same access time (with respect to clock) as valid data transitions. These parameters are not referenced to a specific voltage level but to the time when the device output is no longer driving (for tRPST, tHZ(DQS) and tHZ(DQ)), or begins driving (for tRPRE, tLZ(DQS), tLZ(DQ)). Operating and Timing Figure 10. LPDDR3: tDQSKCKDM timing shows a method to calculate the point when device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.
- 9) Output Transition Timing



- 10) The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as single-ended. The timing parameters tRPRE and tRPST are determined from the differential signal DQS_t-DQS_c.
- 11) Measured from the point when DQS_t/DQS_c begins driving the signal to the point when DQS_t/DQS_c begins driving the first rising strobe edge.
- 12) Measured from the last falling strobe edge of DQS_t/DQS_c to the point when DQS_t/DQS_c finishes driving the signal.
- 13) CKE input setup time is measured from CKE reaching a HIGH/LOW voltage level to CK_t/CK_c crossing.
- 14) CKE input hold time is measured from CK_t/CK_c crossing to CKE reaching a HIGH/LOW voltage level.
- 15) Input set-up/hold time for signal (CA[9:0], CS_n).
- 16) To ensure device operation before the device is configured, a number of AC boot-timing parameters are defined in this table. Boot parameter symbols have the letter b appended (for example, tCK during boot is tCKb).
- 17) The LPDDR3 device will set some mode register default values upon receiving a RESET (MRW) command as specified in "Mode Register Definition".
- 18) The output skew parameters are measured with default output impedance settings using the reference load.
- 19) The minimum tCK column applies only when tCK is greater than 6ns.

16.5 CA and CS_n Setup, Hold and Derating

For all input signals (CA and CS_n) the total t_{IS} (setup time) and t_{IH} (hold time) required is calculated by adding the data sheet $t_{IS}(\text{base})$ and $t_{IH}(\text{base})$ value (see Table 47) to the Δt_{IS} and Δt_{IH} derating value (see Table 49) respectively.

Example: $t_{IS}(\text{total setup time}) = t_{IS}(\text{base}) + \Delta t_{IS}$

Setup (t_{IS}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IH(AC)min}$. Setup (t_{IS}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IL(AC)max}$. If the actual signal is always earlier than the nominal slew rate line between shaded ' $V_{REF(DC)}$ to ac region', use nominal slew rate for derating value (see Figure 15). If the actual signal is later than the nominal slew rate line anywhere between shaded ' $V_{REF(DC)}$ to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see Figure 17).

Hold (t_{IH}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC)max}$ and the first crossing of $V_{REF(DC)}$. Hold (t_{IH}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC)min}$ and the first crossing of $V_{REF(DC)}$. If the actual signal is always later than the nominal slew rate line between shaded 'dc to $V_{REF(DC)}$ region', use nominal slew rate for derating value (see Figure 16). If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to $V_{REF(DC)}$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF(DC)}$ level is used for derating value (see Figure 18).

For a valid transition the input signal has to remain above/below $V_{IH/IL(AC)}$ for some time t_{VAC} (see Table 50).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL(AC)}$ at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL(AC)}$.

For slew rates in between the values listed in Table 49, the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

[Table 47] CA Setup and Hold Base-Values

| unit [ps] | Data Rate | | reference |
|-------------------------|-----------|------|---|
| | 1600 | 1866 | |
| $t_{ISCA}(\text{base})$ | 75 | - | $V_{IH/L(AC)} = V_{REF(dc)} \pm 150\text{mV}$ |
| $t_{ISCA}(\text{base})$ | - | 62.5 | $V_{IH/L(AC)} = V_{REF(dc)} \pm 135\text{mV}$ |
| $t_{IHCA}(\text{base})$ | 100 | 80 | $V_{IH/L(dc)} = V_{REF(dc)} \pm 100\text{mV}$ |

NOTE :

1) ac/dc referenced for 2V/ns CA slew rate and 4V/ns differential CK_t-CK_c slew rate.

[Table 48] CS_n Setup and Hold Base-Values

| unit [ps] | Data Rate | | reference |
|-------------------------|-----------|-------|---|
| | 1600 | 1866 | |
| $t_{ISCS}(\text{base})$ | 195 | - | $V_{IH/L(AC)} = V_{REF(dc)} \pm 150\text{mV}$ |
| $t_{ISCS}(\text{base})$ | - | 162.5 | $V_{IH/L(AC)} = V_{REF(dc)} \pm 135\text{mV}$ |
| $t_{IHCS}(\text{base})$ | 220 | 180 | $V_{IH/L(dc)} = V_{REF(dc)} \pm 100\text{mV}$ |

NOTE :

1) ac/dc referenced for 2V/ns CS_n slew rate and 4V/ns differential CK_t-CK_c slew rate.

[Table 49] Derating values t_{IS}/t_{IH} - ac/dc based AC150

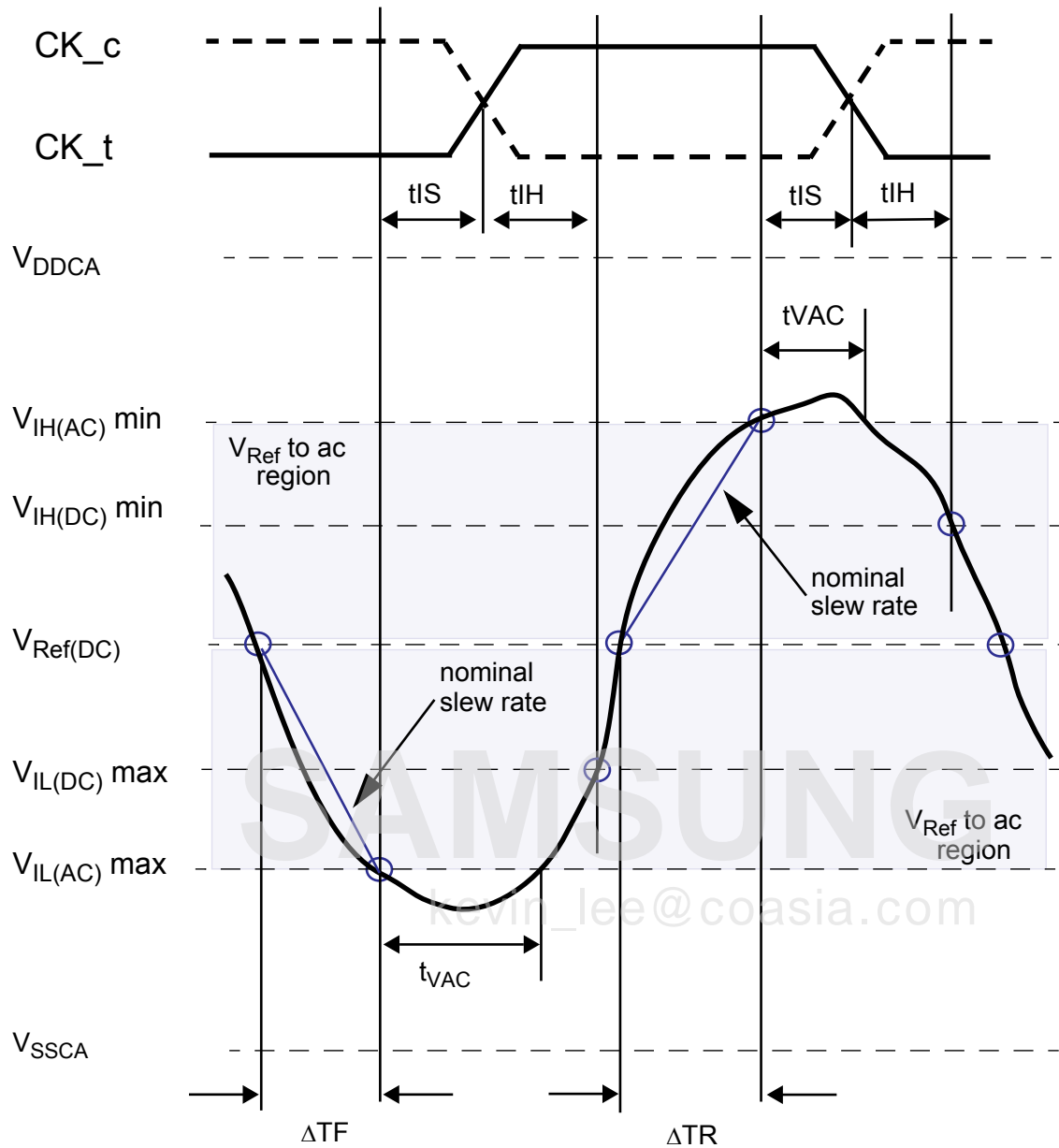
| $\Delta t_{ISCA}, \Delta t_{IHCA}, \Delta t_{ISCS}, \Delta t_{IHCS}$ derating in [ps] AC/DC based AC150 Threshold -> $V_{IH(AC)} = V_{REF(DC)} + 150mV$, $V_{IL(AC)} = V_{REF(DC)} - 150mV$ DC100 Threshold -> $V_{IH(DC)} = V_{REF(DC)} + 100mV$, $V_{IL(DC)} = V_{REF(DC)} - 100mV$ | | | | | | | | | | | | | |
|---|-----|-----------------------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| | | CK_t, CK_c Differential Slew Rate | | | | | | | | | | | |
| | | 8.0 V/ns | | 7.0 V/ns | | 6.0 V/ns | | 5.0 V/ns | | 4.0 V/ns | | 3.0 V/ns | |
| | | Δt_{IS} | Δt_{IH} | Δt_{IS} | Δt_{IH} | Δt_{IS} | Δt_{IH} | Δt_{IS} | Δt_{IH} | Δt_{IS} | Δt_{IH} | Δt_{IS} | Δt_{IH} |
| CA, CS_n Slew rate V/ns | 4.0 | 38 | 25 | 38 | 25 | 38 | 25 | 38 | 25 | 38 | 25 | - | - |
| | 3.0 | - | - | 25 | 17 | 25 | 17 | 25 | 17 | 25 | 17 | 38 | 29 |
| | 2.0 | - | - | - | - | 0 | 0 | 0 | 0 | 0 | 0 | 13 | 13 |
| | 1.5 | - | - | - | - | - | - | -25 | -17 | -25 | -17 | -12 | -4 |

NOTE :

1) Cell contents shaded in red are defined as 'not supported'.

[Table 50] Required time t_{VAC} above $V_{IH(AC)}$ {below $V_{IL(AC)}$ } for valid transition for CA

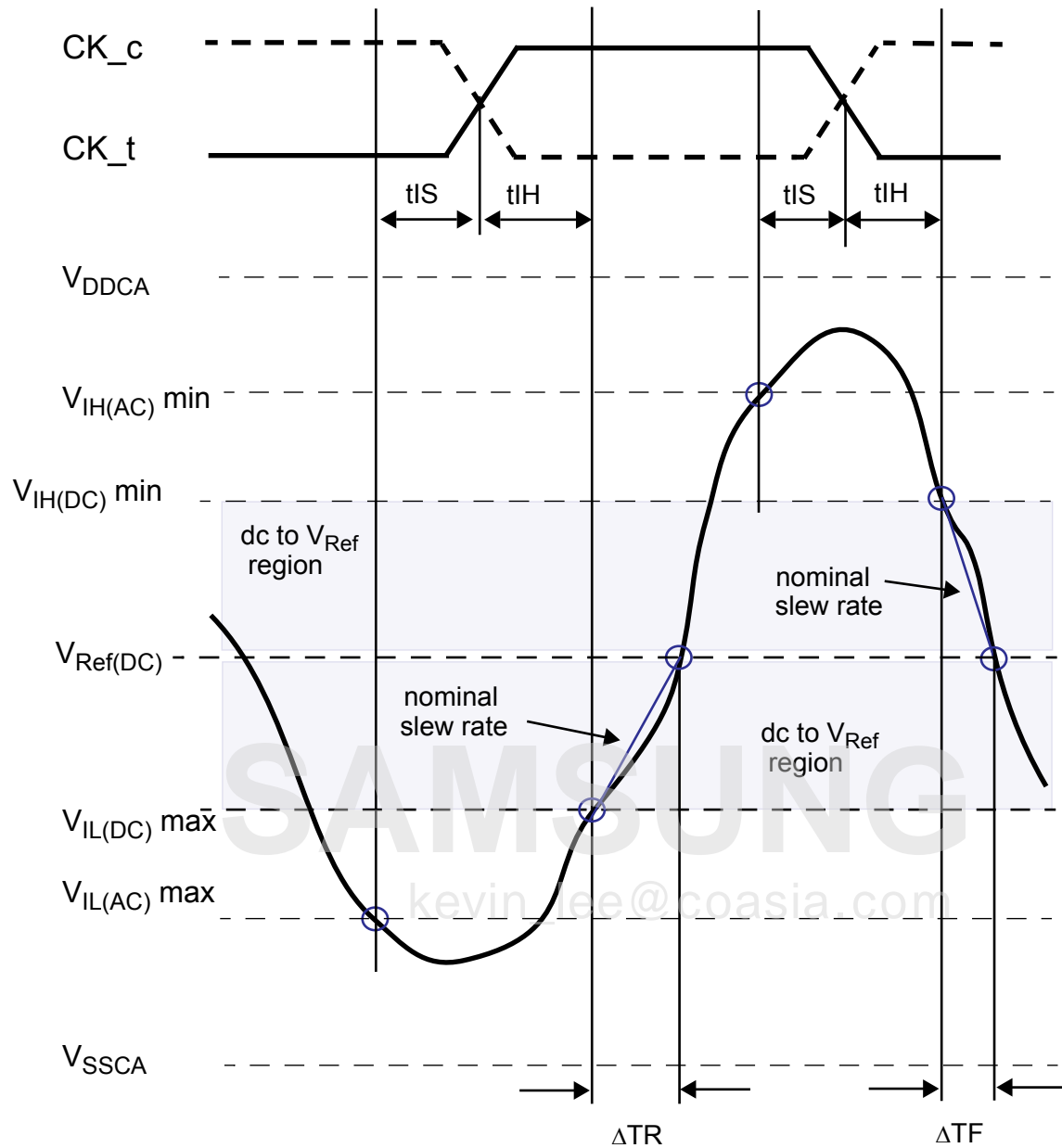
| Slew Rate [V/ns] | t_{VAC} [ps] @ 150mV | | | |
|------------------|------------------------|-----|----------|-----|
| | 1600Mbps | | 1866Mbps | |
| | min | max | min | max |
| > 4.0 | 48 | - | 40 | - |
| 4.0 | 48 | - | 40 | - |
| 3.5 | 46 | - | 39 | - |
| 3.0 | 43 | - | 36 | - |
| 2.5 | 40 | - | 33 | - |
| 2.0 | 35 | - | 29 | - |
| 1.5 | 27 | - | 21 | - |
| < 1.5 | 27 | - | 21 | - |



$$\text{Setup Slew Rate Falling Signal} = \frac{V_{Ref(DC)} - V_{IL(AC) max}}{\Delta TF}$$

$$\text{Setup Slew Rate Rising Signal} = \frac{V_{IH(AC) min} - V_{Ref(DC)}}{\Delta TR}$$

Figure 15. Illustration of nominal slew rate and t_{VAC} for setup time t_{IS} for CA and CS_n with respect to clock.



$$\text{Hold Slew Rate Rising Signal} = \frac{V_{\text{Ref(DC)}} - V_{\text{IL(DC)max}}}{\Delta\text{TR}} \quad \text{Hold Slew Rate Falling Signal} = \frac{V_{\text{IH(DC)min}} - V_{\text{Ref(DC)}}}{\Delta\text{TF}}$$

Figure 16. Illustration of nominal slew rate for hold time t_H for CA and CS_n with respect to clock

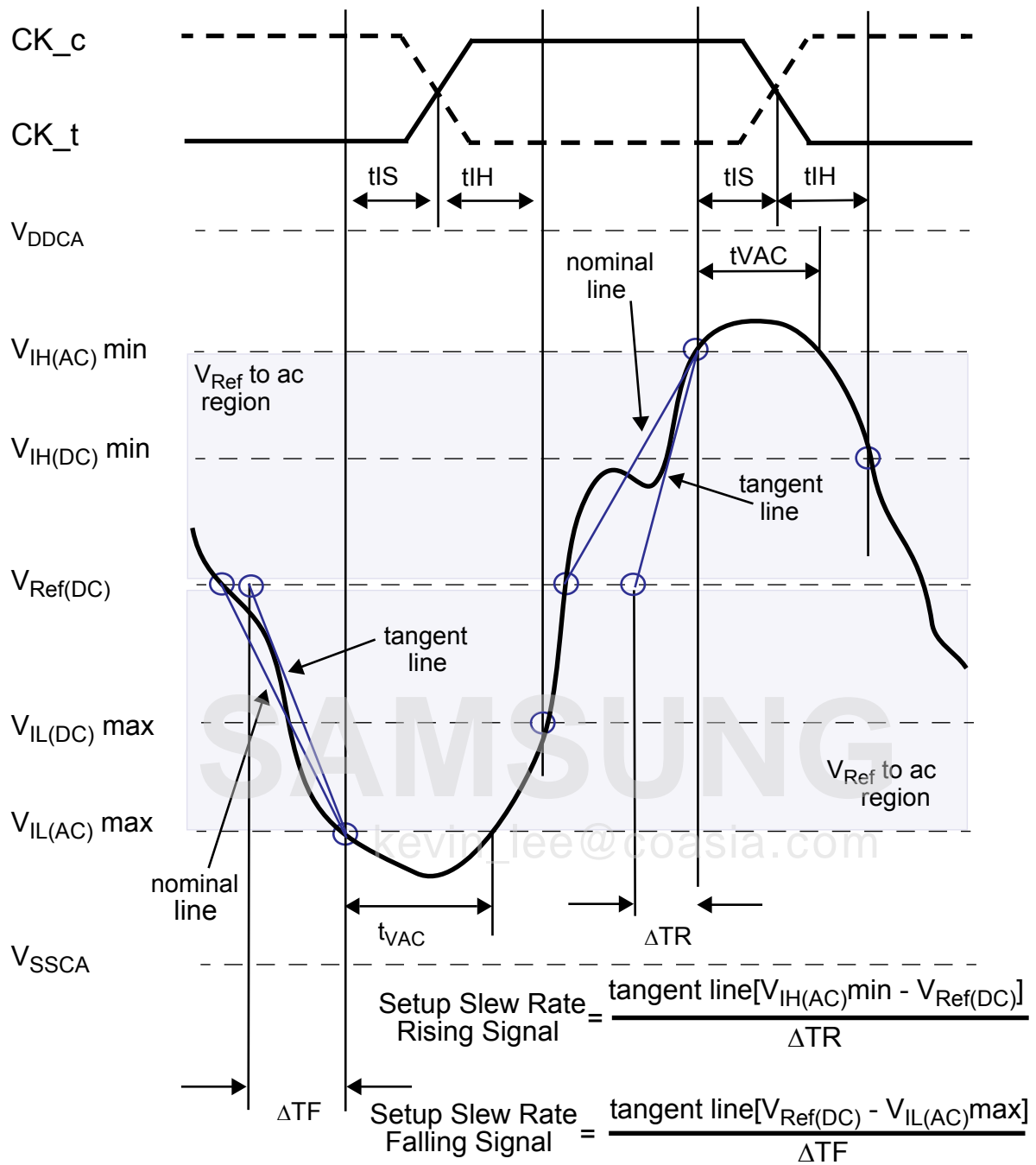


Figure 17. Illustration of tangent line for setup time t_{IS} for CA and CS_n with respect to clock

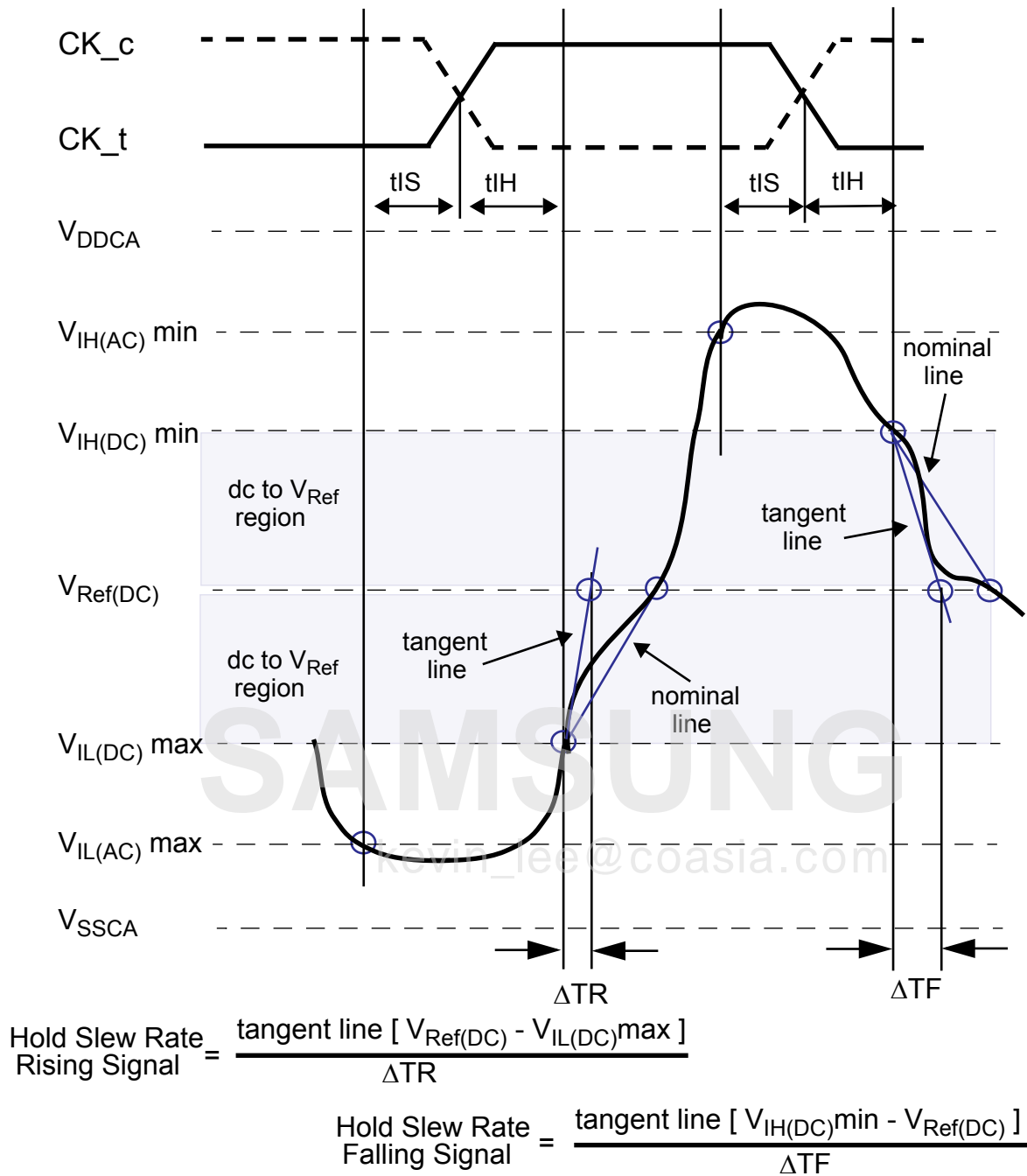


Figure 18. Illustration of tangent line for hold time t_{IH} for CA and CS_n with respect to clock

16.6 Data Setup, Hold and Slew Rate Derating

For all input signals (DQ, DM) the total tDS (setup time) and tDH (hold time) required is calculated by adding the data sheet tDS (base) and tDH(base) value (see Table 51) to the Δt_{DS} and Δt_{DH} (see Table 52) derating value respectively. Example: tDS (total setup time) = tDS(base) + Δt_{DS} .

Setup (tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IH(AC)min}$. Setup (tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IL(AC)max}$ (see Figure 19). If the actual signal is always earlier than the nominal slew rate line between shaded ' $V_{REF(DC)}$ to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded ' $V_{REF(DC)}$ to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see Figure 21).

Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC)max}$ and the first crossing of $V_{REF(DC)}$. Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC)min}$ and the first crossing of $V_{REF(DC)}$ (see Figure 20). If the actual signal is always later than the nominal slew rate line between shaded 'dc level to $V_{REF(DC)}$ region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to $V_{REF(DC)}$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF(DC)}$ level is used for derating value (see Figure 22).

For a valid transition the input signal has to remain above/below $V_{IH/IL(AC)}$ for some time t_{VAC} (see Table 53).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL(AC)}$ at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL(AC)}$.

For slew rates in between the values listed in the tables the derating values may obtained by linear interpolation. These values are typically not subject to production test. They are verified by design and characterization

[Table 51] Data Setup and Hold Base-Values

| [ps] | Data Rate | | reference |
|----------------|-----------|------|--|
| | 1600 | 1866 | |
| $t_{DS(base)}$ | 75 | - | $V_{IH/L(ac)} = V_{REF(dc)} \pm 150mV$ |
| $t_{DS(base)}$ | - | 62.5 | $V_{IH/L(ac)} = V_{REF(dc)} \pm 135mV$ |
| $t_{DH(base)}$ | 100 | 80 | $V_{IH/L(dc)} = V_{REF(dc)} \pm 100mV$ |

NOTE :

1) ac/dc referenced for 2V/ns DQ, DM slew rate and 4V/ns differential DQS_t-DQS_c slew rate and nominal V_{IX} .

[Table 52] Derating values LPDDR3 t_{DS}/t_{DH} - ac/dc based AC150

| $\Delta t_{DS}, \Delta t_{DH}$ derating in [ps] AC/DC based AC150 Threshold $\rightarrow V_{IH(AC)} = V_{REF(DC)} + 150mV, V_{IL(AC)} = V_{REF(DC)} - 150mV$ DC100 Threshold $\rightarrow V_{IH(DC)} = V_{REF(DC)} + 100mV, V_{IL(DC)} = V_{REF(DC)} - 100mV$ | | | | | | | | | | | | | |
|---|-----|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| DQS_t, DQS_c Differential Slew Rate | | | | | | | | | | | | | |
| | | 8.0 V/ns | | 7.0 V/ns | | 6.0 V/ns | | 5.0 V/ns | | 4.0 V/ns | | 3.0 V/ns | |
| | | Δt_{IS} | Δt_{IH} | Δt_{IS} | Δt_{IH} | Δt_{IS} | Δt_{IH} | Δt_{IS} | Δt_{IH} | Δt_{IS} | Δt_{IH} | Δt_{IS} | Δt_{IH} |
| DQ, DM Slew rate V/ns | 4.0 | 38 | 25 | 38 | 25 | 38 | 25 | 38 | 25 | 38 | 25 | - | - |
| | 3.0 | - | - | 25 | 17 | 25 | 17 | 25 | 17 | 25 | 17 | 38 | 29 |
| | 2.0 | - | - | - | - | 0 | 0 | 0 | 0 | 0 | 0 | 13 | 13 |
| | 1.5 | - | - | - | - | - | - | -25 | -17 | -25 | -17 | -12 | -4 |

NOTE :

1) Cell contents shaded in red are defined as 'not supported'.

[Table 53] Required time t_{VAC} above $V_{IH(AC)}$ {below $V_{IL(AC)}$ } for valid transition for DQ, DM

| Slew Rate [V/ns] | t_{VAC} [ps] @ 150mV | | | |
|------------------|------------------------|-----|----------|-----|
| | 1600Mbps | | 1866Mbps | |
| | min | max | min | max |
| > 4.0 | 48 | - | 40 | - |
| 4.0 | 48 | - | 40 | - |
| 3.5 | 46 | - | 39 | - |
| 3.0 | 43 | - | 36 | - |
| 2.5 | 40 | - | 33 | - |
| 2.0 | 35 | - | 29 | - |
| 1.5 | 27 | - | 21 | - |
| < 1.5 | 27 | - | 21 | - |

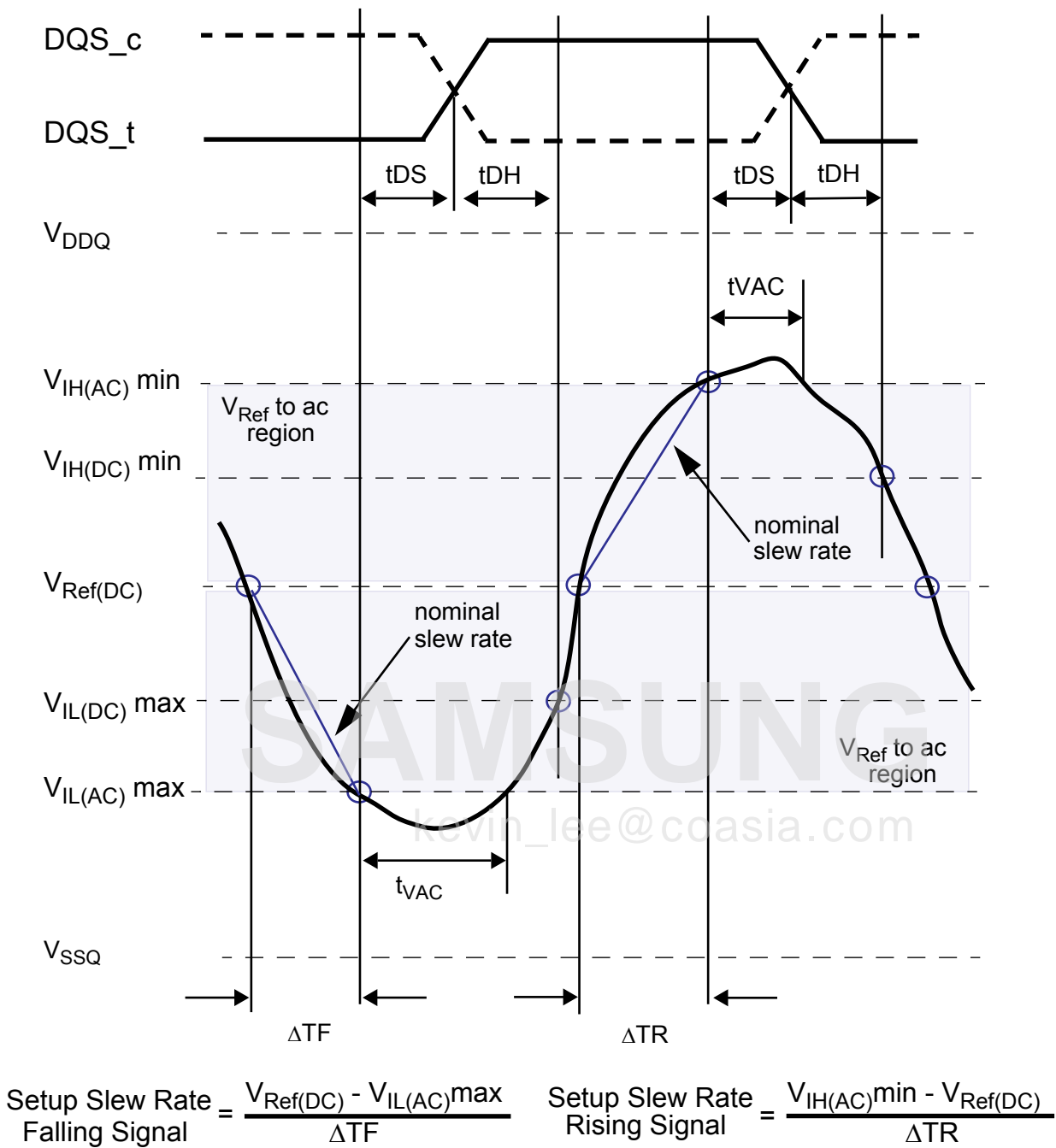
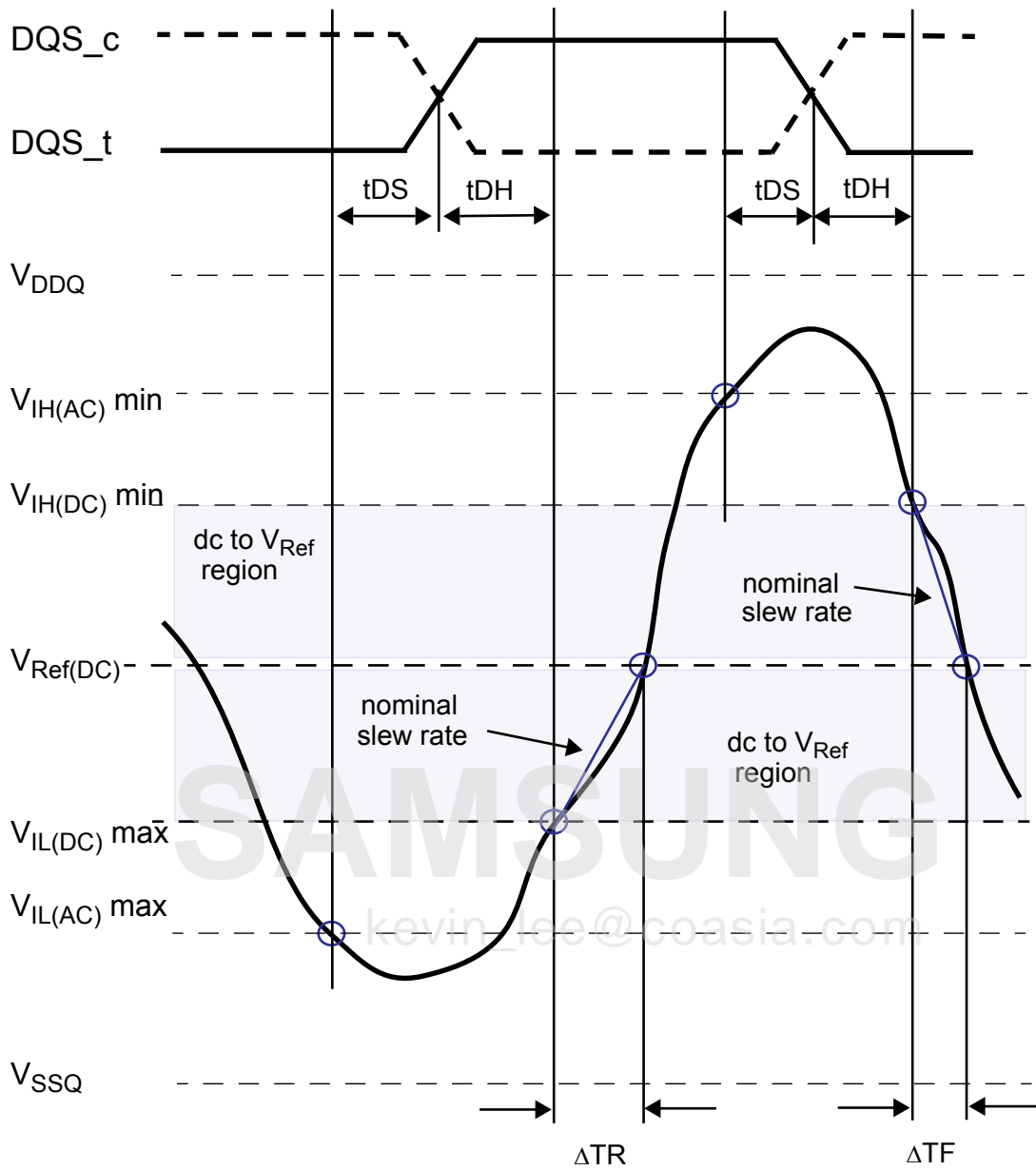


Figure 19. Illustration of nominal slew rate and t_{VAC} for setup time t_{DS} for DQ with respect to strobe



$$\text{Hold Slew Rate Rising Signal} = \frac{V_{Ref(DC)} - V_{IL(DC)max}}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{V_{IH(DC)min} - V_{Ref(DC)}}{\Delta TF}$$

Figure 20. Illustration of nominal slew rate for hold time t_{DH} for DQ with respect to strobe

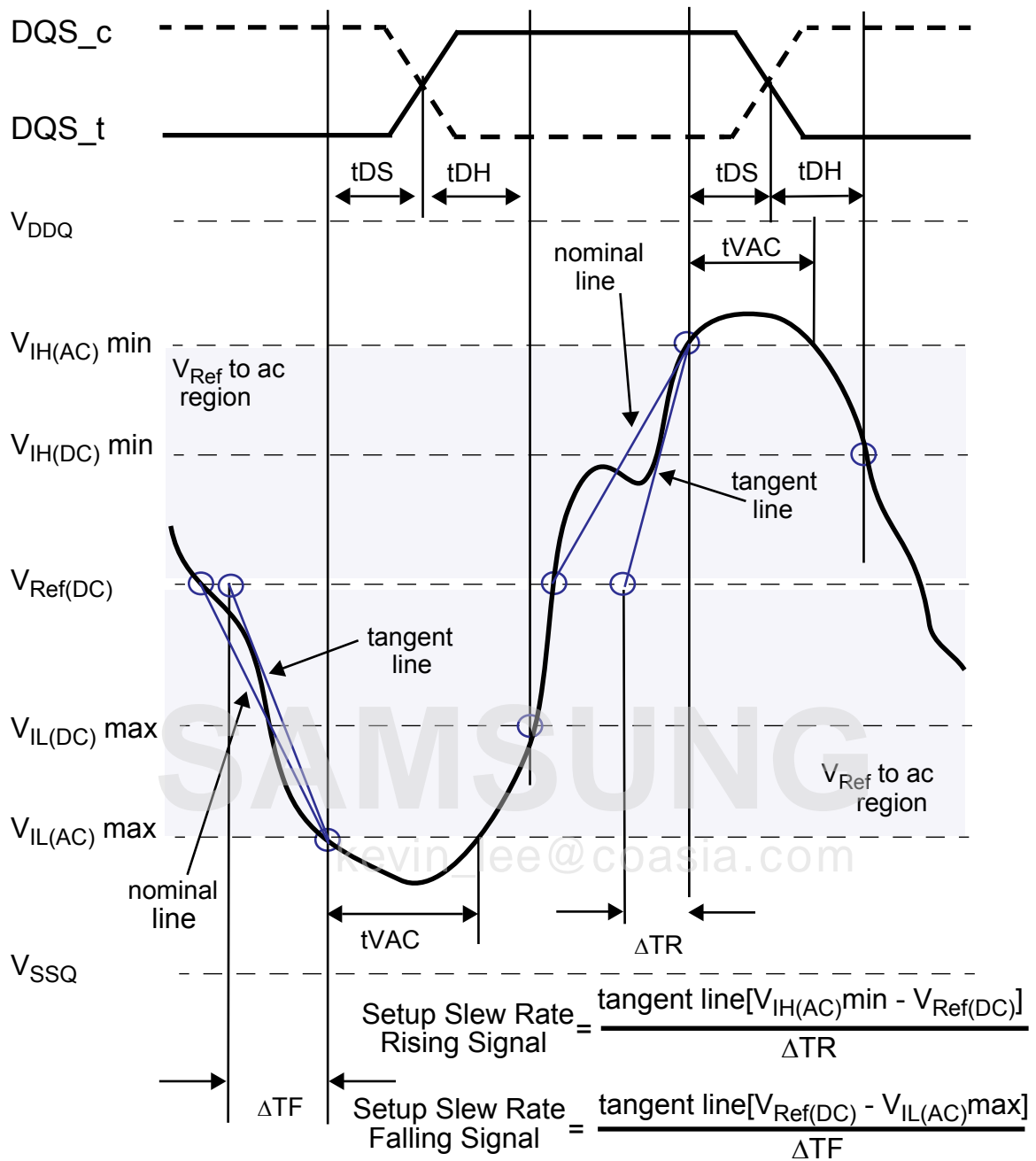


Figure 21. Illustration of tangent line for setup time t_{DS} for DQ with respect to strobe

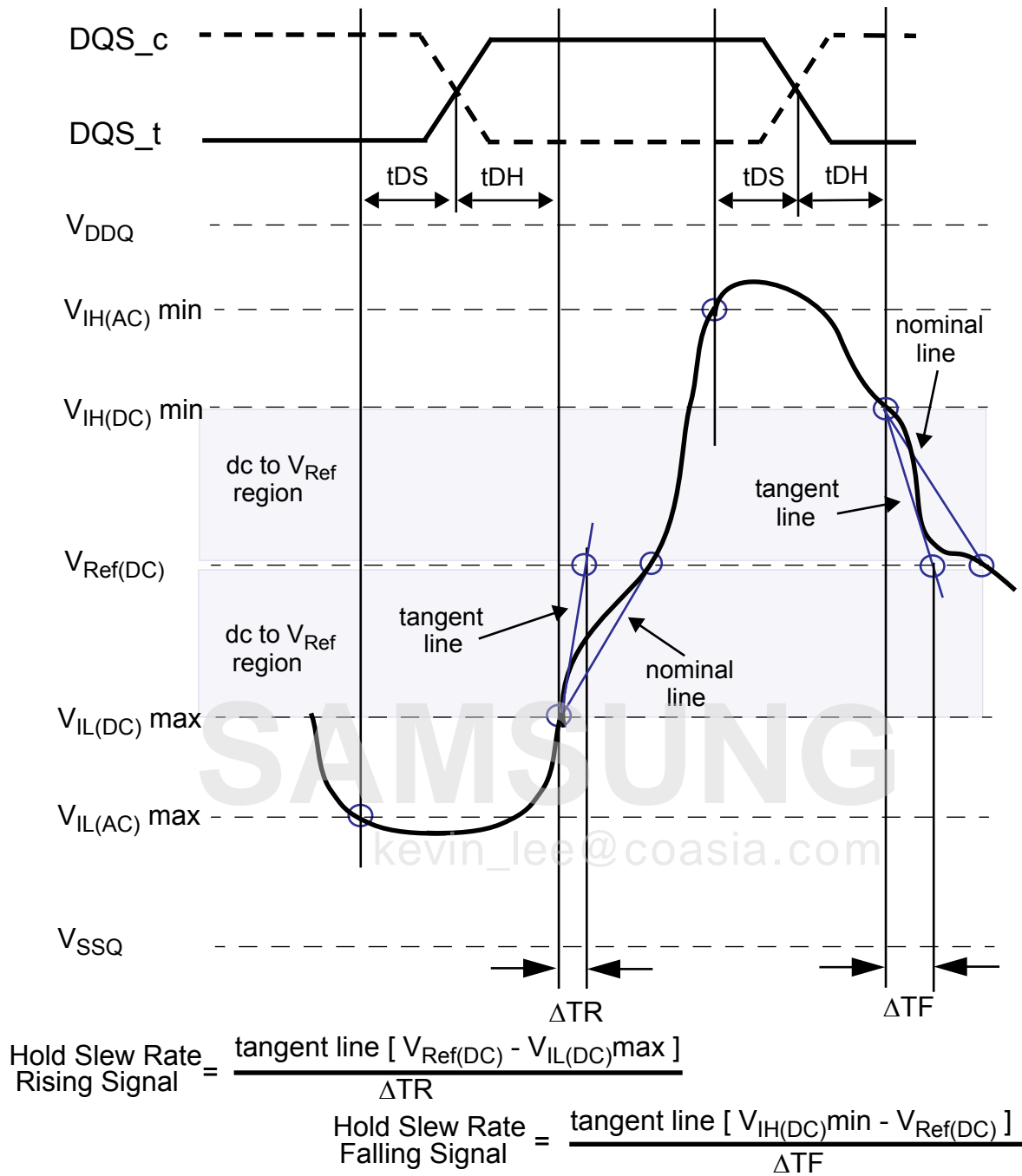


Figure 22. Illustration of tangent line for hold time t_{DH} for DQ with respect to strobe